Resistive Switching Devices for Memory Selectors, Memory Cells & RF Switches

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NEW CLASSES OF SEMICONDUCTING MATERIALS

Amorphous chalcogenide and oxide semiconductors (and their crystalline counterparts) offer wide potential application to emerging electronics technology. These materials are leading candidates for memory selectors ($GeTe_6$, SiTeAsGe [STAG], $TaHfO_x$), phase change memory cells (PC-RAM: GeSbTe [GST] and Al-GST), Oxide Resistive memory (RRAM: HfO_x, TaO_x) and RF switch elements (GeTe), among others. What is attractive about these materials is that they can reversibly change electrical conductivity over many orders of magnitude. In some cases, this change is non-volatile (but reversible) as in GST for PC-RAM or HfOx for RRAM. In other cases, this change is temporary (i.e. volatile) as in the case of $GeTe_6$ or $TaHfO_x$ for selector applications. In this latter case, removal of electrical stimulus returns the material to is high resistivity state.

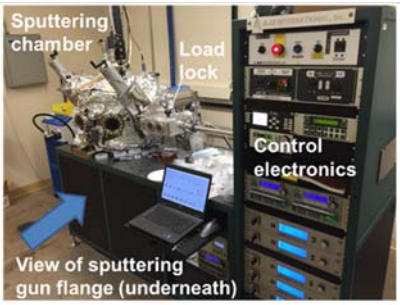

Figure 1: Deposition system at CMU for making threshold switches.

While some of this behavior is reasonably well understood, much remains unclear. For example, the nature of the selector volatile ON-state has been difficult to study as it is a transient phenomenon. Additionally, interface electronic states of these materials when in contact with electrodes, the dynamics of the volatile and non-volatile transformations, including the initiating and the rate-controlling processes are all understood in a very limited way. With understanding of these processes and materials physics will come the ability to control these properties of interest.

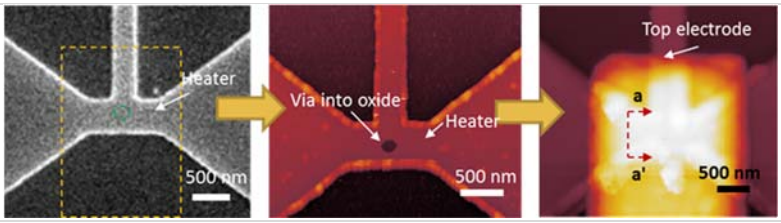

Figure 2: An example of a nanoscale two-terminal device with an integrated heater for multi-modal interrogation (simultaneous V and T inputs).

Work in this project uses a specifically designed 11-target chalcogenide and oxide sputter deposition system that co-deposits alloy films from elemental targets (Figure 1) to develop and study resistive alloys as a function of composition. The focus of the work is on understanding their fundamental material properties. Special purpose scaled test structures are fabricated to measure electrical and structural properties at high speed and temperature. Figure 2 shows an example of a test structures made at CMU for applying simultaneous 5 ns thermal and electrical pulses to GST for measuring high speed crystallization dynamics. Additional modalities are using optical and magnetic stimuli to extract fundamental transport properties as a function of composition.

NOVEL DEVICE APPLICATIONS

As noted above, these materials enable many device applications, from non-linear selectors to memory cells to RF switches. Work in this research area examines the links between material properties and device performance in an attempt to optimize devices. For example, Figure 3 on the next page shows studies of nanoscale HfOx devices where the hysteretic I-V behavior is compared to structural changes within the device. Crystallization during the switching process is revealed. Similarly, Figure 4 shows an RF switch developed at CMU using GeTe as the switching material and a patterned W heater as the actuation element. Issues that have emerged from this work include the breakdown voltage of the materials as it limits power handling of the switches. Both of these represent new functionality that will be available in future electronic systems and must be optimized for functionality and performance.

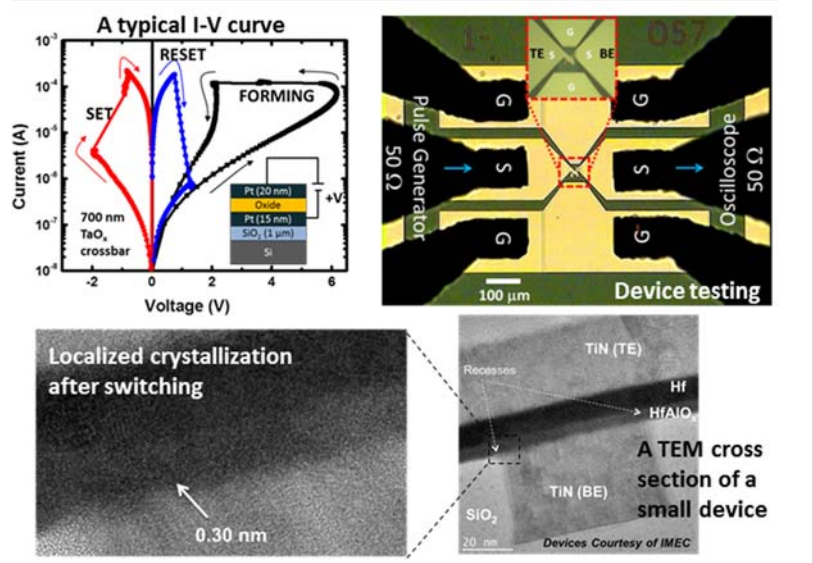

Figure 3: Resistive switching (typical I-V curve) from devices fabricated and tested at CMU (device testing). Insight are sought at the electrical and structural level. Images are transmission electron microscope images of device after operation.

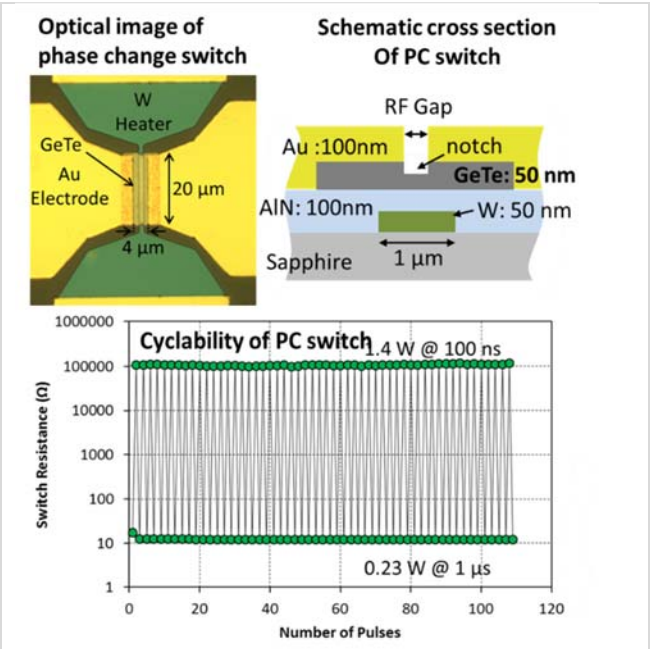

Figure 4: RF switches fabricated and tested at CMU that employ GeTe as the switching material and a patterned W heater to control the state of the material.

Selected Relevant Publications:

Some recent publications of are attached for reference. These include description of the technique of using high speed electrical thermometry to characterize these devices [1] and [2], and the development of high speed external heaters [3], as well as the use of these techniques to study heating events and structural changes in devices [4]. These papers also detail demonstrations of devices for advanced electronic systems like relaxation oscillators arrays [5], the development of the RF switch [6] and its use to create reconfigurable RF systems [7].

[1] M. Noman, A. A. Sharma, Y. Lu, M. Skowronski, P. A. Salvador, and J. A. Bain, "Transient characterization of the electroforming process in TiO2 based resistive switching devices," *Appl. Phys. Lett.*, vol. 102, no. 2, p. 023507, Jan. 2013.

[2] A. A. Sharma, M. Noman, M. Skowronski, and J. A. Bain, "High-speed in-situ pulsed thermometry in oxide RRAMs," in *Proceedings of Technical Program - 2014 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)*, 2014, pp. 1–2.

[3] M. Xu, G. Slovin, J. Paramesh, T. E. Schlesinger, and J. A. Bain, "Thermometry of a high temperature high speed micro heater," *Review of Scientific Instruments*, vol. 87, no. 2, p. 024904, Feb. 2016.

[4] J. Kwon *et al.*, "Transient Thermometry and High-Resolution Transmission Electron Microscopy Analysis of Filamentary Resistive Switches," *ACS Appl. Mater. Interfaces*, vol. 8, no. 31, pp. 20176–20184, Aug. 2016.

[5] A. A. Sharma *et al.*, "Low-power, high-performance S-NDR oscillators for stereo (3D) vision using directly-coupled oscillator networks," in *2016 IEEE Symposium on VLSI Technology*, 2016, pp. 1–2.

[6] N. El-Hinnawy *et al.*, "12.5 THz Fco GeTe Inline Phase-Change Switch Technology for Reconfigurable RF and Switching Applications," in *2014 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2014, pp. 1–3.

[7] R. Singh *et al.*, "A 3/5 GHz reconfigurable CMOS low-noise amplifier integrated with a four-terminal phase-change RF switch," in *2015 IEEE International Electron Devices Meeting (IEDM)*, 2015, p. 25.3.1-25.3.4.

Transient characterization of the electroforming process in TiO_2 based resistive switching devices

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The transient electroforming process of TiO_2-based resistive switching devices is investigated using a pulsed voltage method, and the electroforming time is found to vary from 10^{-8} s to 10^{-1} s as function of pulse magnitude (3–8 V) and ambient temperature (25–100 °C). Pulsed experiments and thermal simulations reveal that Joule self-heating has a significant effect on the electroforming dynamics, specially for electroforming voltages above 5.5 V where there is little dependence on ambient temperature and the electroforming time (10–100 ns) is much shorter than the device thermal time constant (≈2 μs). © *2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4776693]

Resistance switching devices based on many different transition metal oxides, such as TiO_2, TaO_2,[1] NiO,[2] $SrTiO_3$,[3,4] HfO_2,[5] etc, are being extensively studied for their potential in non-volatile memory-related applications. This class of devices is generally referred to as resistance random access memories (RRAM). The devices usually exhibit two resistance states and one can switch between these states by applying electrical bias to the device. The geometry of the device in most cases is a simple metal/oxide/metal heterostructure, making them quite simple to fabricate and integrate with other processes. Although these devices have been under intensive study for over a decade, much remains unknown about the exact physical processes that govern their operation. Many different mechanisms have been proposed,[6] but none, at this point, is able to conclusively explain all the physical phenomena observed.

In the as-fabricated state, most RRAM devices do not exhibit resistance switching behavior. To obtain stable resistance switching conditions, they must undergo an initialization process known as "electroforming." Electroforming is usually carried out by performing a DC voltage sweep until a sudden decrease in device resistance is observed. This is a one-time event, which is believed to induce formation of conductive filaments in the oxide layer that lower the device resistance and participate in the resistance switching phenomenon.[7] While this DC electroforming method is effective, it provides almost no insight into the physical process or the parameters that are responsible for controlling this event. Here, we have used a pulse-forming method that allows us to examine the dynamics of the process. Using this method, we are able to observe the transient voltage, current, and power dissipation of the device during the forming process. Along with the dynamics, we have characterized the correlation between the electroforming voltage, time, and the ambient temperature. We also correlated the electroforming conditions to the subsequent resistance switching properties of the device.

In order to carry out this study, we fabricated crossbar type devices based on TiO_2 as the functional oxide, as shown in Fig. 1(a). For the bottom electrode (pad B in Fig. 1(a)), 5 nm Ti (for adhesion) and 15 nm Pt layers were sputter deposited on a Si substrate pre-coated with 1 μm of thermal SiO_2. The metal layers were then patterned using photolithography and Ar ion milling. Then, a 15 nm thick TiO_2 layer was deposited by atomic layer deposition at 200 °C using a $Ti(NMe_2)_4$ precursor with an O_2 plasma oxidation step; and again patterned using photolithography and Ar ion milling in order to expose the contact pads for the bottom electrode. Finally, a 20 nm thick Pt top electrode (pad A) layer was deposited using DC sputtering and patterned using a lift-off process. The overlap of the top and the bottom electrodes defines the device size, which is approximately $5 \times 5\ \mu m^2$. A third metal pad (C) adjacent to A and B was created during the bottom electrode fabrication step in order to facilitate high speed electrical testing as will be explained below. A large array of these devices was fabricated to carry out the electroforming experiments under various temperature and biasing conditions.

The device geometry was designed such that both DC and high speed pulsing experiments could be performed on the same structure. For simple DC experiments (performed using Keithley 2400 source-meter), pads A and B are used to access the top and bottom electrodes of the device, respectively. For high speed experiments (performed using an Agilent 81110 A pulse generator and a DSO6104A oscilloscope), two GS-type microwave probes are used on pad pairs A-C and B-C as shown in Fig. 1(b). The inset shows the electrical schematic of this setup. Pad pair A-C is used to supply the voltage pulse to the device and pair B-C is used to monitor the transmitted pulse to the oscilloscope. This setup essentially creates a series circuit containing the RRAM device and the termination resistance of the oscilloscope, which is set to 50 Ω to match the impedance of the microwave probes

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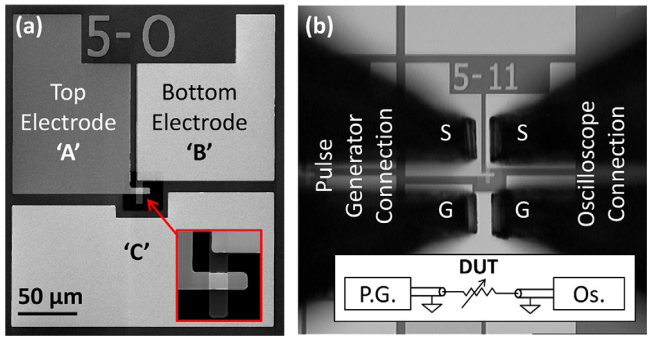

FIG. 1. (a) Scanning electron micrograph of the $5 \times 5\,\mu m^2$ crossbar device; (b) Electrical connection for pulsed electroforming measurements and schematic of measurement circuit (inset).

and the cables connecting the instruments to the device. Since voltage pulses of known amplitude can be generated from the pulse generator, by monitoring the portion of the pulse transmitted to the oscilloscope, voltage drop and the current through the device can be precisely determined as a function of time, as they evolve during the pulse.

Under DC voltage sweeps, these devices exhibit bipolar switching behavior with a threshold voltage of approximately ± 2 V as shown in Fig. 2. Prior to obtaining this repeatable switching behavior, the devices must be electroformed. When electroforming is performed with DC voltage sweeps, a current compliance of 5 mA is enforced and a sudden resistance decrease is generally observed around 4 volts. Using the high-speed measurement setup described above, three types of pulsed experiments were performed to investigate electroformation in detail. For clarity of explanation, they will be referred to as "fixed pulse width," "fixed pulse amplitude," and "pulse train" experiments. For the "fixed pulse width" experiment, pulse widths were set to a specific value (e.g., 50 ns, 100 ns, 250 ns, etc.) while the amplitude was increased in increments of 0.1 V between consecutive voltage pulses (with a gap of $\approx$1 s between each pulse). Fig. 3(a) shows the voltage across a device as a function of time for a selected set of 250 ns long pulses leading up to the

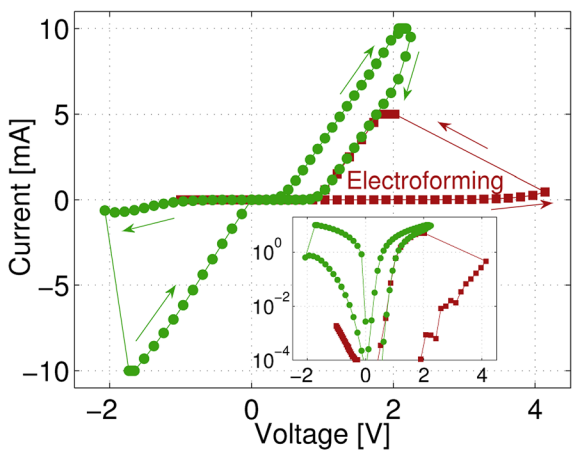

FIG. 2. Current-voltage characteristics of a $5 \times 5\,\mu m^2$ TiO_2 based device displaying resistive switching behavior under DC voltage sweep (green curve with circles). Prior to switching, a positive DC voltage sweep is performed in order to induce electroforming (red curve with squares). Current compliance of 10 mA and 5 mA are enforced during switching and electroforming, respectively. The inset shows the two curves in logarithmic scale.

electroformation event. In this plot, t = 0 corresponds to the time when the pulse reaches its full amplitude (after the initial rise time of 2.5 ns). Once a pulse with sufficient amplitude is applied, the device resistance suddenly changes to a low value (P5 in Fig. 3(a)). Since the device is in series with two 50 Ω resistors (the input impedance of the pulse generator and the termination impedance of the oscilloscope), as the resistance of the device decreases with time, the voltage across the device also shows a corresponding drop. The time corresponding to the inflection point of the electroforming voltage curve is denoted as $t_{forming}$, which marks the time it takes to initiate permanent lowering of the device resistance. The voltage at $t_{forming}$ is denoted as $V_{forming}$ (these values are both marked in Fig. 3(a)). Additionally, when the pulse amplitude was kept below the electroforming pulse, subjecting the device to multiple sweeps of voltage pulses did not seem to alter the device response in any permanent way. In other words, P1 through P4 in Fig. 3(a) were repeatable as long as the device did not experience P5.

The instantaneous power dissipation of the device during the pulse is shown in Fig. 3(b). Beginning from t = 0, the power dissipation steadily increases with time as the device resistance drops, and a very sudden increase is observed as the device goes through the electroforming process. After this non-reversible change, the resistance of the device usually stabilizes in the range of 150 Ω–250 Ω; lower resistance generally corresponds to a higher $V_{forming}$, and vice versa.

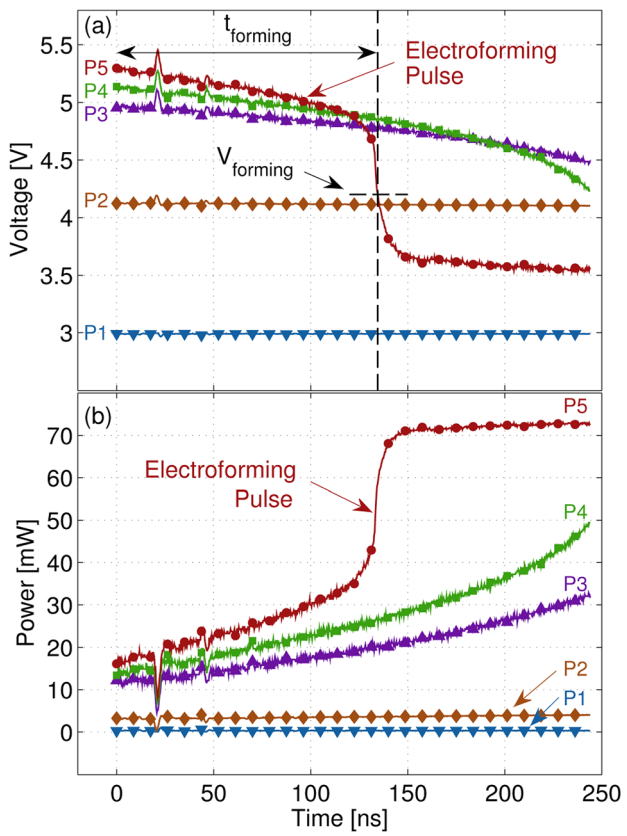

FIG. 3. (a) Voltage across the device as a function of time for 250 ns pulses (at $T_{amb} = 25\,^{\circ}C$) with increase amplitude (from P1 to P5) leading up to the electroforming pulse. P3-P5 are consecutive pulses, however not all pulses between P1 and P3 are shown. Inflection point on the electroforming pulse (red closed circles) is defined as $t_{forming}$ and $V_{forming}$; (b) Power dissipation as a function of time corresponding to each pulse in (a).

Once the device resistance stabilizes, the power dissipation also reaches a stable value, as can be seen in the 150–250 ns time range in Fig. 3(b) for the electroforming pulse.

Given the procedure of this experiment, it is possible that $t_{forming}$ and $V_{forming}$ may have been influenced by all the pulses the device experienced prior to the electroforming pulse. To directly test for this possibility, "fixed pulse amplitude" experiments were performed. Here, each pristine untested device was subjected to a single voltage pulse of fixed amplitude with a width that would, based on the prior results, lead to electroformation. This test protocol was then repeated for several different voltage amplitudes, and at three different ambient temperatures (T_{amb}), 25 °C, 62.5 °C, and 100 °C (established by controlling the stage temperature of the probe station) to check the influence of temperature on electroforming characteristics. For each voltage amplitude and T_{amb} combination, we repeated the test on three separate devices to check the uniformity of $t_{forming}$ across different devices.

Fig. 4 shows $t_{forming}$ as a function of $V_{forming}$ for all three T_{amb} conditions. Considering the $T_{amb} = 25$ °C case first, it is clear that as long as $V_{forming}$ is greater than approximately 4.5 volts, $t_{forming}$ rises roughly exponentially as $V_{forming}$ decreases. However, a much more drastic increase in $t_{forming}$ is observed for $V_{forming} < 4.5$ V. It is remarkable that $t_{forming}$ increases by almost five orders of magnitude when $V_{forming}$ decreases from 4 V to 3.8 V. The same type of behavior is observed for higher T_{amb} conditions as well. However, as the ambient temperature increases, the voltage at which the drastic $t_{forming}$ increase is observed shifts toward lower $V_{forming}$. As discussed earlier, once the electroforming event is complete, the power dissipation as a function of time reaches a steady value. Fig. 4 also shows the post-electroformed power level as a function of $V_{forming}$ for each of these devices.

After electroforming the devices with these single voltage pulses, DC voltage sweeps were conducted to examine their switching behavior. Devices with $V_{forming} < 5.5$ volts (corresponding to post electroformed power < 150 mW) were found to be switchable, while those above this threshold were permanently stuck in a low resistance state. This is not unexpected since high $V_{forming}$ leads to very large power dissipation immediately after electroforming, likely causing permanent damage to the filaments responsible for switching.

Similar electroforming studies have recently been reported by Lee *et al.*, on $SrTiO_x$, TiO_y, and NiO_z based devices,[8,9] which yielded qualitatively similar results in terms of the $t_{forming}$ dependence on pulse amplitude. In addition to monitoring the $t_{forming}$, our approach allows for examining the role of device temperature during the process. From Fig. 4, it is apparent that when $V_{forming}$ is low, increasing ambient temperature from 25 °C to 100 °C can lower $t_{forming}$ by many orders of magnitude. However, the lack of the obvious ambient temperature dependence at higher voltages does not mean the events at higher $V_{forming}$ are not thermally driven. Our data will be used below to demonstrate that thermal events are important at all forming voltage levels.

Since TiO_2 is semiconducting, the conductivity of the device should increase as the temperature increases due to power dissipation. An increased conductivity, or decreased device resistance, should lower the measured voltage over the device due to the series configuration of the circuit. The decrease in voltage observed in the early part of the electroforming voltage profile (e.g., from 0–100 ns in Fig. 3(a)) is likely due to this phenomenon. Similar voltage decreases are observed under all electroforming conditions. However, since the device current prior to electroforming is a highly non-linear function of voltage (as seen in Fig. 2), the magnitude of this effect greatly diminishes under low voltage conditions (e.g., pulses P1 and P2 in Fig. 3(a)) since the power dissipation level is significantly lower.

Assuming this is a thermal phenomenon, the voltage decrease should cease after the device reaches thermal steady state. Fig. 5 shows the voltage versus time for a 10 μs pulse prior to electroformation. The voltage monotonically decreases for $\approx$2 μs and then reaches a steady state value. This suggests that the thermal time constant, τ, of our devices is roughly 2 μs. We performed transient thermal simulations (using COMSOL MULTIPHYSICS) on a structure that has the same area and structure as our devices (shown in the inset of Fig. 5). For the simulation, a constant power was

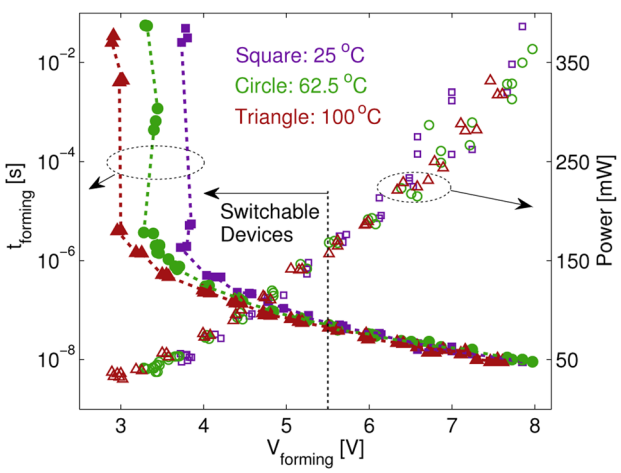

FIG. 4. Electroforming time (left vertical axis, closed symbols) and post-electroforming power (right vertical axis, open symbols) as a function of electroforming voltage at three different ambient temperatures. Repeatable resistance switching was only exhibited by devices for which post electroforming power was less than 150 mW ($V_{forming} < 5.5$ V).

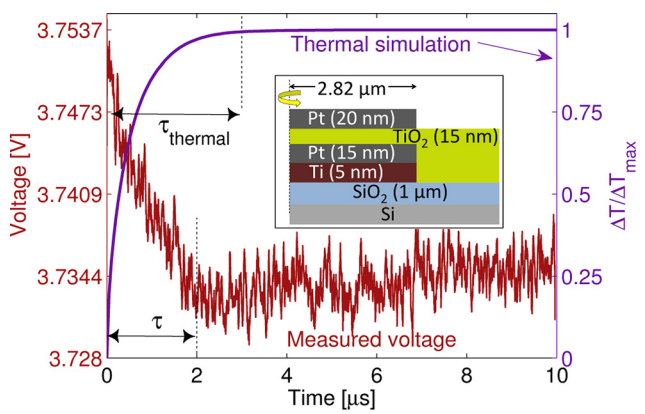

FIG. 5. Transient measurement (left vertical axis) of the voltage across a device subjected to a 10 μs pulse prior to electroforming. Estimated time constant, τ, until the voltage stabilizes is $\approx$2 μs. Simulated curve (right vertical axis) shows normalized temperature rise as function of time (implemented in COMSOL MULTIPHYSICS). The thermal time constant, $\tau_{thermal}$, is $\approx$3 μs. A 2-D axial symmetric model with device area equal to 5×5 μm^2 device was used (inset).

applied to the device beginning at t = 0 s. Fig. 5 shows the normalized temperature increase as a function of time. The thermal time constant, $\tau_{thermal}$, for this structure is approximately ≈3 μs, which is close to the experimental value described above. Physically, this time constant is a direct result of the thermal conductance and heat capacity of the underlying 1 μm thick SiO_2 layer ($k_{SiO2} = 1.3$ W/(m K), $C_{SiO2} = 733$ J/(kg K) used in the simulation). These combined observations suggest that the initial voltage decrease observed during the electroforming pulse is largely driven by Joule heating. This interpretation of device heating is consistent across all of our data, whether or not steady state is achieved, even down to electroforming times of less than 10 ns.

To confirm that heating is significant even for short electroforming pulses, we performed a set of "pulse train" experiments. Here, pulse trains containing fixed number of pulses (of specific pulse widths and amplitudes) with precise time gap (t_{gap}) among them were applied to the device to trigger electroforming. The pulse amplitude was increased in increments of 0.1 V (with ≈1 s gap between consecutive pulse trains) until electroforming was observed. Fig. 6 shows the result where trains of 100 pulses having 100 ns widths were applied to trigger electroforming, where t_{gap} ranged from 3 μs to 3 ns. It was found that for $t_{gap} > 2$ μs, $V_{forming}$ approaches the same value as a single 100 ns pulse (estimated from 25 °C case in Fig. 4, indicated by upper dotted line in Fig. 6). However, as t_{gap} is reduced below 2 μs, $V_{forming}$ starts to decreases rapidly. For the minimum possible t_{gap} (3 ns for our equipment), $V_{forming}$ is very close to the value for a single 10 μs long pulse (estimated again from Fig. 4, indicated by lower dotted line in Fig. 6). This observation is reasonable since 100 × 100 ns = 10 μs. Similar experiments with pulse trains containing varying number of pulses and durations also revealed the same result. In general, $V_{forming}$ decreased with $t_{gap} < 2$ μs and approached a value corresponding to $V_{forming}$ of a single long pulse with total duration of all the individual pulses. In other words, when t_{gap} is less than the thermal time constant of the system, the effects of consecutive pulses begin to accumulate; under these conditions, the device does not have enough time to cool down from the prior pulse. The smooth transition from single pulse to the aggregated pulse train indicates that heating is a controlling feature of the electroforming process for all pulses, even the shortest ones, where thermal steady state is not reached. The large sensitivity to ambient temperatures at low forming voltage and the insensitivity to the ambient temperature at the high biases remains a question for further study.

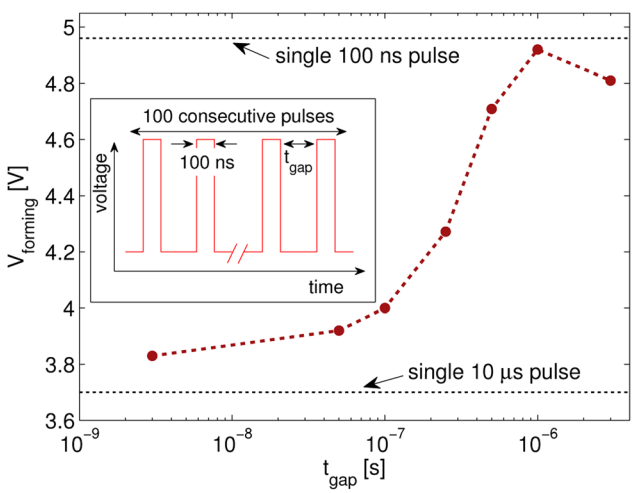

FIG. 6. Electroforming with pulse trains consisting of 100 consecutive 100 ns pulses with t_{gap} time interval between each pulse. Upper and lower dotted lines represent the electroforming voltages for a single 100 ns and 10 μs wide pulses, respectively.

It should be noted that a subtlety of the measurements was that $V_{forming}$ for the pulse trains at large t_{gap} values (i.e., nominally independent pulses) consistently fell slightly below the single pulse value. This might be the result of cumulative subtle damage to the oxide that would only become significant after thousands of pulses. This experiment was not structured to examine this effect in detail, but it may be an important avenue to explore when investigating RRAM cyclability.

In summary, close examination of the transients during the electroforming process, induced using voltage pulses, reveals that temperature plays a critical role in determining the electroforming voltage and time for TiO_2 based RRAM devices at all voltage levels. For low electroforming bias, the effect of ambient temperature is very pronounced, and it can change the electroforming time by many orders of magnitude. Thermal simulations and "pulse train" experiments indicate that, at higher electroforming bias, Joule heating plays a dominant role in determining the electroforming characteristics, but the ambient temperature is less important. More work is necessary in order to precisely determine the temperature at the onset of electroforming. Avoiding high power dissipation immediately after the completion of the electroforming process is necessary in order to preserve the resistance switching ability of the devices, as only devices formed with relatively low powers were switchable.

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High-Speed In-situ Pulsed Thermometry in Oxide RRAMs

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Various mechanisms for forming and switching in oxide based RRAMs have been proposed, based on first principle and Monte-Carlo simulations [1]-[3]. However, the thermal kinetics are often overlooked in absence of any well-established temperature measurement technique. Previous attempts at temperature extraction utilized specialized test structures that may have a thermal environment very different from the actual devices [4]. Here, we present an in-situ thermometry technique for TaO_x based RRAM in both the pre-forming and post forming regimes. It must be noted that this technique is applicable to any material system where self-heating is a factor. DC-IV sweeps usually involve significant self-heating due to high localized power dissipation. Thus we use high–speed pulses in a time domain transmissometry (TDT) setup to eliminate any self-heating in the device to obtain true temperature calibrations. This thermometry technique allows us to extract the local temperatures within the device using the material properties themselves as a thermometer and define the geometry of the heat source i.e. the conducting filament (CF) radius.

Methodology & Calibration

The devices considered in this study are crossbar structures with 20 nm thick electrodes and 60 nm thick reduced TaO_x as the functional oxide layer. The devices electroform and switch reliably as shown in Fig. 1. The device size considered was 5×5 μm^2 in order to prevent any size limited observations. Fig. 2 shows the RF probe positioning and the inset shows the high-speed TDT setup used to calibrate the temperatures in the samples. We first calibrate the temperature dependent I-V in the pre-formed devices followed by low and high resistance states (LRS & HRS) post-forming. In TDT, pulses are launched from a pulse generator (terminated with 50 Ω) into a 2.92 mm RF cable (50 Ω transmission line). The device is connected in series with the signal path resulting in a reflected pulse moving towards the generator and a transmitted pulse moving towards an high sampling rate oscilloscope which is also terminated at 50 Ω. Knowing the transmitted voltage and the input, we can determine the transmission coefficient and subsequently the voltage and current transients across the device.

In order to calibrate the temperature dependence of the device I-V, without any self-heating, we deliver 5 ns long pulses of increasing amplitudes and sample the first 1 ns to generate the pulsed I-V plots as shown in Fig. 3. The pristine devices (pre-forming) display a thermal time constant of 2.5 μs [5] and hence the device does not undergo any self-heating in the first 1 ns. These pulsed I-V characteristics are then measured as a function of ambient temperature to yield the true temperature dependent I-V devoid of any self-heating. In the pre-formed state, the device conducts uniformly and hence any current non-uniformity (like filamentation) requires separate temperature calibration. As the LRS and HRS have different conducting areas, we have to recalibrate the I-V-T curves, for both states after forming. It must be noted that the smallest thermal time constant during switching is ~120 ns. Hence, we sample only the first 340 ps of the pulse. Thus, we can generate the temperature dependent I-V for both the LRS and HRS.

Temperature Extraction

The temperature at each point in the forming and switching I-V sweeps of Fig. 1 is determined by mapping each I-V point to a unique temperature using the calibration curves shown in Fig. 3, 4 and 5.

The temperature rise during the electroforming process before any localization occurs increases from room temperature up to 50 °C before showing filamentary conduction. At this point, the temperature calibration in Fig. 3 no longer holds true. Hence the temperature excursions can be much higher in the remainder of the forming process (locally, well above 700 °C at high biases, to facilitate vacancy migration). However, we can still know that the point at which the conduction becomes non-uniform in terms of voltage, current and temperature. For Fig. 1, it happens at 5 V, ~100μA and 50 °C.

Similarly, we apply the temperature calibration from Fig. 4 & 5 to LRS and HRS I-Vs respectively. Temperature excursions for a DC sweep of the switch are shown in Fig. 6, with T for the LRS shown in (a), the I-V plot itself in (b) and T for the HRS in (c). Again, the temperature reaches 515 ºC on the onset of RESET eventually reaching 445 ºC upon completion; during SET the temperature goes from 125 ºC to 385 ºC.

Filament Size Extraction

The knowledge of temperature enables us to estimate the geometry of the heat source. For DC measurements, the temperature rise is approximately proportional to the dissipated power with a proportionality constant of the thermal resistance (R_{th}). Fig. 7 plots temperature rise versus steady state electrical power dissipated in the device in LRS and HRS. The slopes of Fig. 7 are determined by the thermal resistance between the place where the heat is being generated and thermal ground. The fact that the ΔT vs. power plots pass through the origin indicate correct interpretation of temperature and heat source. Note that linear sections of these curves that do not extrapolate through the origin represent transitional states where the size of the heated zone is changing with power.

To estimate the degree of power localization reflected by the different slopes in Fig. 7, we compute the thermal resistance of a filamentary hot zone as a function of filament radius. A schematic of the simulation and the parameters chosen are shown in Fig. 8, with the R_{th} computed from these simulations plotted in Fig. 9 as a function of filament radius. Changing the geometry of the CF from cylindrical to conical does not affect the results of the simulation. Based on thermal conductivities and interface conductance (independently measured using frequency domain thermo-reflectance), the filaments are extremely narrow (a 10 nm radius agrees with R_{th} ~ 6 K/μW) at low power in both states (HRS and LRS), but the heat generation zone at the switching voltage extends 0.5 - 1 μm in radius around the filament (R_{th} ~ 0.14-0.4 K/μW, respectively for HRS and LRS). Moreover, the slope of the ΔT vs. P plot for forming yields a R_{th} of ~ 0.03 K/μW which corresponds to a heat source with a size equal to the device dimensions, consistent with the conducting area predicted by the plot shown in Fig. 9.

Conclusion

In summary, we present an in-situ temperature characterization technique applicable to forming as well as switching in oxide RRAM. This work provides unambiguous evidence that the switching event in these oxide systems includes a thermal event involving temperature excursions of hundreds of ºC within a 10 nm filament. The applicability of this technique to as-fabricated devices makes it distinct from previous extraction methodologies that make use of specialized test structures that may have very different thermal environment compared to functional memory blocks. One of the key contributions of this technique is the scalability of this technique with changing size of the conducting filament.

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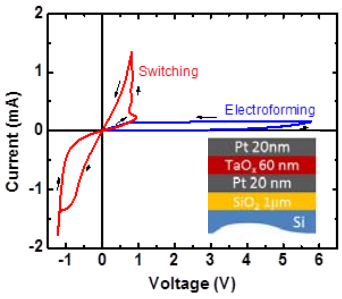

Figure 1: Forming and switching curves with device stack as inset

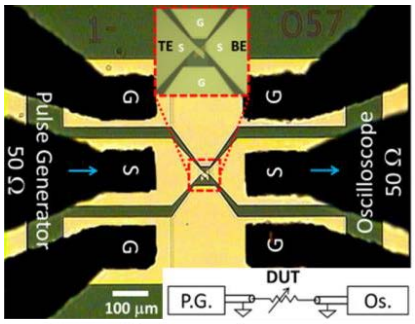

Figure 2: Optical photo of devices showing GSG RF probe points in a TDT setup (inset)

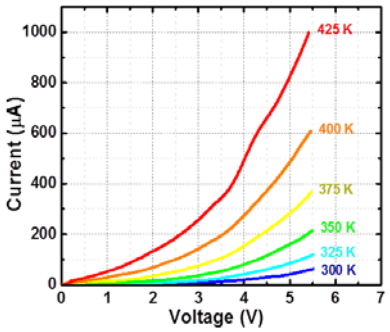

Figure 3: The pulsed I-V curves for the virgin states of the device (prior to electroforming).

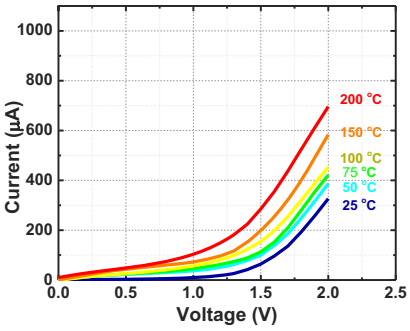

Figure 4: The pulsed I-V curves for the high resistance state (HRS) of switch.

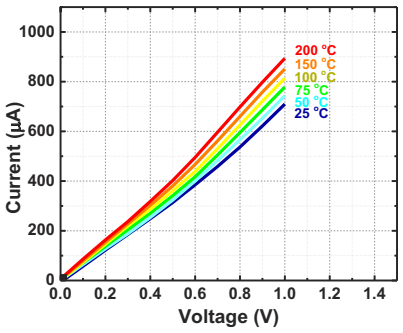

Figure 5: The pulsed I-V curves for the low resistance state (LRS) of the switch

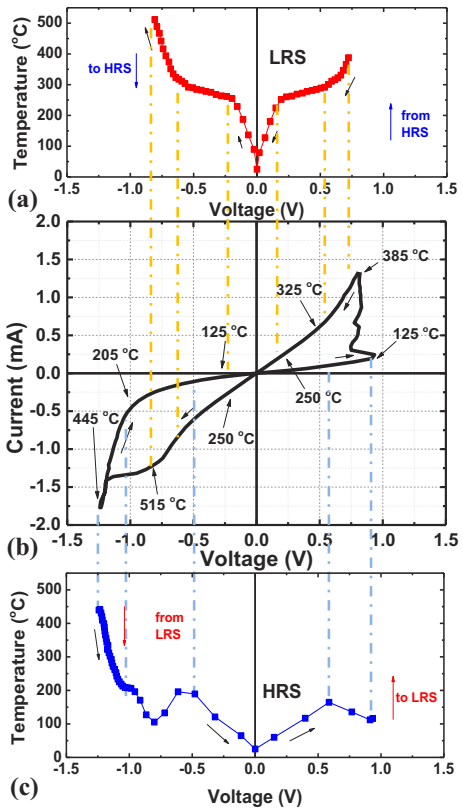

Figure 6: The temperature rise during a DC sweep of (a) the LRS and (c) the HRS extracted from (b) I-V data for the switch. The calibrations shown in Figures 3 and 4 were used to generate these figures.

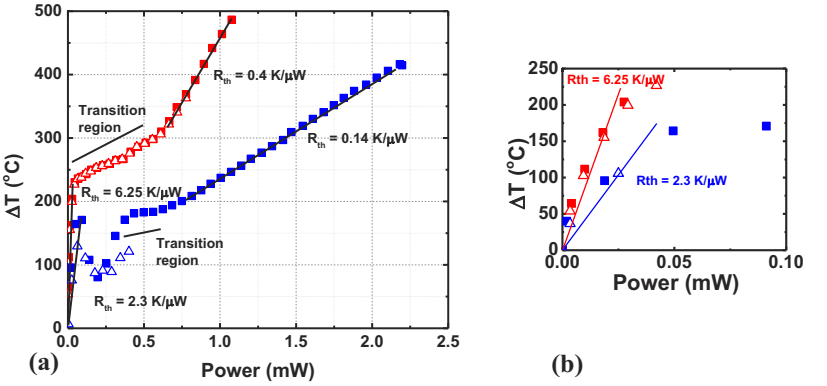

Figure 7: (a) Temperature rise versus dissipated power revealing regions of different thermal resistance, R_{th}, defined as the ratio of temperature rise to power dissipated. (b) Magnified view of the low power region indicating geometry of heat source

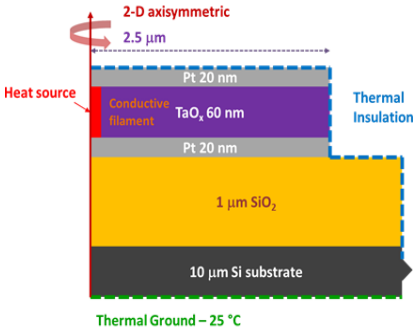

Figure 8: A schematic of the thermal simulation done to estimate the degree of thermal localization during switching. Heat assumed to be dissipated in CF

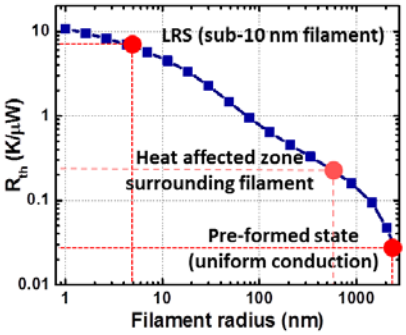

Figure 9: A plot of R_{th} vs filament radius for the simulation shown in Figure 8. Red spots indicate the filament radius corresponding to the device in pre-formed and post-formed states

Thermometry of a high temperature high speed micro heater

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A high temperature high-speed tungsten micro heater was fabricated and tested for application in phase change switches to indirectly heat and transform phase change material. Time domain transmissometry was used to measure heater temperature transients for given electrical inputs. Finite element modeling results on heater temperature transients show a good consistency between experiments and simulations with 0.2% mismatch in the best case and 13.1% in the worst case. The heater described in this work can reliably reach 1664 K at a rate of 1.67×10^{10} K/s and quench to room temperature with a thermal RC time constant (time for T to fall by a factor of e) of less than 40 ns. © *2016 AIP Publishing LLC.* [http://dx.doi.org/10.1063/1.4942249]

I. INTRODUCTION

Micro heaters of dimensions less than 100 μm are used in many applications including sensors,[1–5] calorimeters,[6,7] lithography,[8] and data recording.[9–15] Micro heaters are also employed in applications such as phase change (PC) materials characterizations,[16,17] PC memory devices,[9,14,15] and PC switches in reconfigurable circuits.[18,19]

In PC switch applications, phase change material is transformed between the amorphous (high resistance—OFF) state and the crystalline (low resistance—ON) state. To switch phase change material, such as GeTe, into the "OFF" amorphous state it must be heated above its melting temperature (1000 K) and then cooled quickly (typically with thermal RC time constant less than 100 ns) to below the crystallization temperature.[20–23] To put the same material into the "ON" state is less demanding since heating to a temperature below the melting point along with a duration time longer than 30 ns can be sufficient to crystallize the material.[21] Thus to take the PC material into the amorphous state requires greater electrical power to achieve higher temperatures as well as switch design that permits cooling in a time constant shorter than 100 ns to prevent crystallization. This process places the greater constraints on the electrical drive as well as the switch architecture. A heater physically separated from the switch can be used to turn the switch on or off by producing a desired temperature and time profile.[19] The heater must be capable of being driven, with sufficient power at high speed so that one can reach temperatures above 1000 K and cool sufficiently fast. If the heater is modeled as a first order system consisting of a parallel thermal resistance (R_{th}) and thermal capacitance (C_{th}), then cooling will follow an exponentially decaying temperature profile with a time constant, $\tau = R_{th}C_{th}$. For phase change switch applications, this value of τ must be on the order of 100 ns. Previous work has shown heater designs which are either capable of reaching temperatures above 1000 K[5,10,13] or to cool in less than 1 μs.[12,16,17] However, previously reported heaters are not able to meet both of these requirements.

In this paper, we demonstrate a micro heater with a tungsten thin film heating element. Tungsten was chosen for the heater material due to its high melting point and good thermal stability.[24,25] We used a sapphire substrate to provide good heat sinking since sapphire is an electrical insulator with a reasonably high thermal conductivity (35 W/(m K) at room temperature).[26] In this paper heater geometry is described and demonstrated to reach temperatures above 1600 K while having a thermal RC time constant, τ of less than 100 ns. In addition we show that this heater has very good stability, with less than 0.1% change in resistance over 10 000 pulses.

II. METHODS

A. Device geometry, modeling, and fabrication

The geometry of the heater is carefully chosen to meet the design specifications within the limitation of testing equipment and fabrication process. The maximum voltage that can be delivered to the heater is limited by the capability of the pulse generator (below 10 V). So for generating a given temperature, the voltage required should be minimized. A simple back-of-the-envelope analysis shows that required voltage is given by $V = \sqrt{TR/R_{th}}$, where T is temperature, R is electrical resistance of the heater, and R_{th} is thermal resistance between the heater and the ambient (bottom of substrate). Since R increases while R_{th} decreases with heater length, reducing heater length will reduce the required voltage for a given temperature. On the other hand, minimizing heater width will minimize the heated volume of substrate and thus reduce the thermal capacitance and speed up the device thermal response. Thus, heater width is chosen to be 1 μm, which is the minimum feature size in our lithography process using contact mask aligner. Heater length is chosen to be 5 μm taking account of alignment tolerance in the future process of aligning 1 μm wide PC device to the center of the heater.

In Fig. 1(a), we present the structure of the heater which consists of a 55 nm thick layer of tungsten on top of a

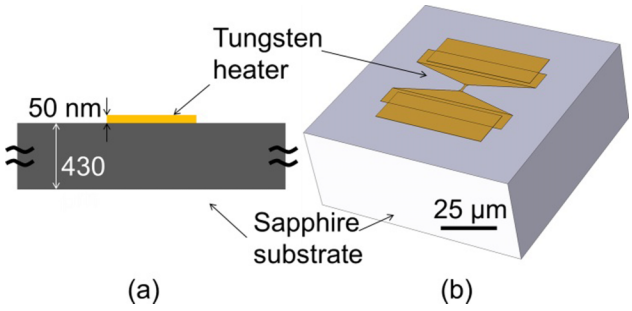

FIG. 1. (a) Cross-sectional view of the device (b) COMSOL perspective view of the device. The modeled dimensions of substrate ($100\,\mu m \times 100\,\mu m \times 40\,\mu m$) are smaller than the actual dimensions ($25\,400\,\mu m \times 25\,400\,\mu m \times 430\,\mu m$) but large enough to eliminate any substrate size effects.

430 μm thick sapphire substrate. The heater is 1 μm wide and 5 μm long and includes leads and pads for landing probes. The heater was produced by depositing a well-oriented 55 nm thick tungsten layer by DC sputter on the sapphire substrate and patterning using photolithography and reactive ion etching (RIE). X-ray rocking curves about the (110) reflection showed a full-width half-maximum of 0.5°. A second 100 nm thick tungsten layer for the contact pads was deposited in the same way and patterned using a lift-off process. Fig. 1(b) shows a perspective view of the heater. To model the heater operation we constructed a finite element simulation (COMSOL) using the measured dimensions of a fabricated heater and a $100\,\mu m \times 100\,\mu m \times 40\,\mu m$ bulk sapphire substrate. The modeled substrate is large enough to ensure simulation results independent of substrate size.

Fig. 2 shows an optical microscope and SEM image of the heater. The central part of the heater, which is shown as part A in Fig. 2(b), has a width of 0.93 μm. While the transition regions, which are shown as part B in Fig. 2(b), have width that increases from 0.93 μm to 2.08 μm gradually. The model calculation was based on the actual measured dimension of the heater rather than the design parameters as shown in Fig. 2(b). Also incorporated into the model was the resistance of section A and B as heater strip resistance R_H, while the resistance of part C is considered as heater lead resistance R_L. Fig. 2(c)

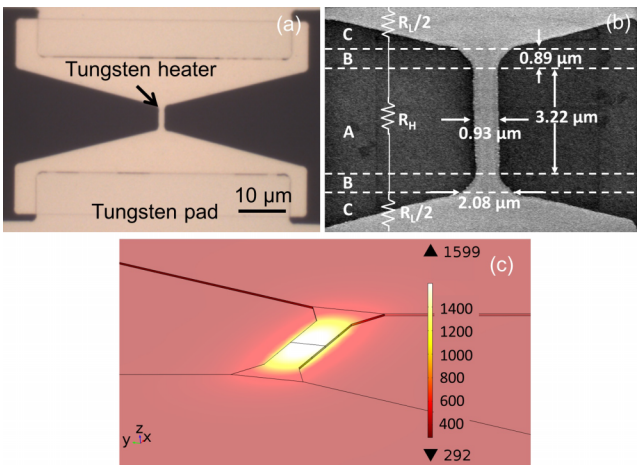

FIG. 2. (a) Optical microscopic image (left view) of the device and (b) SEM image (right view) of the heater region with measured dimensions of each feature. (c) Perspective view of the simulated temperature map of the heater.

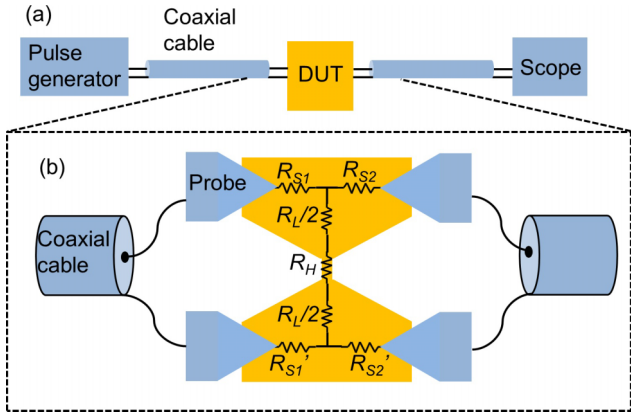

FIG. 3. (a) Setup for TDT measurement circuit. (b) Schematic for parasitic resistance of device in TDT measurement.

shows the perspective view of the simulated temperature map of whole structure with input voltage pulse of 5 V 100 ns. The details about pulse measurement and corresponding simulation will be discussed in Subsections II B–II E.

B. Measurement setup

We employed time domain transmissometry (TDT) using the arrangement shown in Fig. 3(a) to measure the temperature of the heater. A pulse generator with a 50 Ω output resistance and an oscilloscope with a 50 Ω input resistance were connected to RF probes through two 2.92 mm coaxial cables. The RF probes made contact on two sides of the pads as shown in Fig. 3(b). After a voltage pulse is launched from the pulse generator to the heater, the heater temperature rises via joule heating. The heater resistance also rises due to the linear dependence of the resistance on temperature. The temperature coefficient of resistance (TCR) of tungsten is known to be constant over the entire temperature range below the melting point.[24,25] Thus, by knowing the resistance change of the heater, we can infer the temperature of the heater. We measured the transmitted voltage as a function of time resulting from the incident voltage pulse using the oscilloscope. From the transmitted voltage, we can calculate the heater resistance as a function of time. We then infer the temperature of the heater as a function of time using the TCR of the heater.

To accurately extract the temperature from the measured voltage pulse, we need to know the parasitic series resistances $R_{S1} + R'_{S1}$ and $R_{S2} + R'_{S2}$ and the heater strip resistance R_H as shown in Fig. 3(b). These parasitic series resistances originate in the resistance of cables and probes as well as contact resistance between probes and pads. Fig. 4 shows the circuit used for measuring parasitic resistances. A source meter and an oscilloscope are connected to two sides of the device as shown in Figs. 4(a) and 4(b). The difference between Figs. 4(a) and 4(b) is the value of the input impedance of the oscilloscope. By changing this load resistance from 50 Ω to 1 MΩ, we can write Equations (1) and (2) below where R_{M1} to R_{M4} is the resistance measured from the source meter,

$$R_{M1} = R_{S1} + R'_{S1} + (R_H + R_L) \| (R_{S2} + R'_{S2} + 50), \quad (1)$$

$$R_{M2} = R_{S1} + R'_{S1} + R_H + R_L. \quad (2)$$

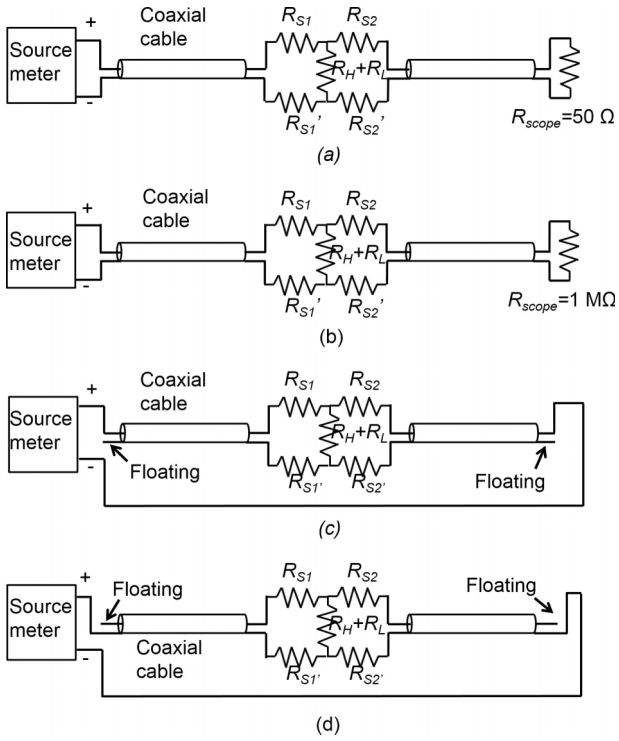

FIG. 4. Testing circuits for parasitic resistance measurement.

In Equation (2), since $R_H + R_L$ is around 20 Ω, we can assume it is much less than 1 MΩ.

In Figs. 4(c) and 4(d), the signal side and the ground side of the cables are floating, and we can write

$$R_{M2} = R_{S1} + R'_{S1} + R_H + R_L, \tag{3}$$

$$R_{M4} = R'_{S1} + R'_{S2}. \tag{4}$$

Combining the four equations, we can solve for $R_{S1} + R'_{S1}$ and $R_{S2} + R'_{S2}$.

To determine the exact heater strip resistance R_H, we performed a four-point DC measurements on 5 devices with the same pad size and 1 μm heater width but different heater lengths ranging from 1 μm to 20 μm. By linearly fitting the resistance data as a function of heater length and finding the y-axis intercept, we can determine the lead resistance R_L and calculate the heater resistance R_H. Since R_H is more than 60% of the total resistance of the device, more than 60% of the power will be dissipated in the heater strip with a small volume of 0.25 μm^3. The power density in the heater strip is 80 times more than that in the other parts of the device. Thus, it is reasonable to assume that the heater strip is the only part that is heated up and R_H is the resistance that changes with temperature as well as time.

A key parameter that must be determined and is required to determine the temperature of the heater is the TCR of the tungsten thin film. To determine this, a van der Pauw structure of an identically deposited tungsten sheet film with the same thickness as the heater layer was heated from 25 °C to 105 °C with an interval of 10 °C using a heated chuck. Measurement was not performed in higher temperatures due to the limited range of the heated chuck. At each temperature, we performed four-point sheet resistance measurement on this sample. We determined the TCR of the tungsten by taking the slope of the plot of $(R_\square - R_{\square 0})/R_{\square 0}$ versus ΔT, where $R_\square$ is the sheet resistance at temperature T, $R_{\square 0}$ is the sheet resistance at room temperature, and ΔT is the temperature difference with respect to room temperature. Based on Ref. 25, it is reasonable to assume the TCR is constant over larger temperature range and can be used to infer temperature from room temperature to tungsten's melting temperature.

C. Simulation

We simulated the TDT measurement in COMSOL to model and verify our measurement. We modeled the 3-D heater device using measured values for thickness and heater dimensions as determined from fabricated devices. We used three coupled physics modules in COMSOL to simulate the system response: (i) electrical circuit, (ii) heat transfer, and (iii) electrical current. For the electrical circuit simulation, the nodes and components are defined such that it matches the circuit in Figure 3. For the heat transfer simulation, we set the bottom of the substrate to be room temperature (293 K). The rest of the exposed boundaries are set to be in thermal isolation. The initial condition for temperature is 293 K in all domains. We set the entire heater domain to be the joule heating heat source. For the electrical current simulation, we set the two ends of the heater pads to be nodes in electrical circuit simulation. The initial condition for voltage is 0 V in all domains. We used the temperature dependent thermal conductivity and heat capacity at constant pressure of sapphire as provided by Refs. 26 and 27, respectively. The resistivity of the heater layer tungsten thin film was measured to be 143 ± 1 nΩ m at room temperature by four-point measurements on van der Pauw structures. This is much higher than the bulk value (55 nΩ m),[25] but similar to the reported value (121 nΩ m) for 60 nm thin film.[28] From the simulation, we obtained the expected voltage drop that would be observed across the oscilloscope, the spatial average temperature for the heater region, the lumped heater resistance, and the temperature distribution along the length of the heater. By comparing simulated and measured oscilloscope voltage and the lumped heater resistance, we calculated that mismatches for both cases are smaller than 2%. Thus, we determined that our model was sufficiently accurate to predict the heater behavior.

D. Temperature extraction

We established a temperature extraction method to extract lumped average temperatures of the heater as a function of time based on the parameters determined above and the transmitted pulse. The heater resistance $R_{H,\Delta T}$ at a temperature that is $\Delta\overline{T_{eff}}$ above room temperature is given by

$$R_{H,\Delta T} = R_H\left(1 + \alpha\,\Delta\overline{T_{eff}}\right), \tag{5}$$

where α is the tungsten TCR. For this method to be valid, a constant TCR is required over the entire temperature range of interest. Refs. 24 and 25 show that the TCR of tungsten is constant even over temperatures close to the melting point.

Since the device is in parallel with the oscilloscope, the parallel resistance R_P is

$$R_P = (R_{H,\Delta T} + R_L) \| (R_{S2} + R'_{S2} + 50). \quad (6)$$

Thus, the total DC resistance seen from the input node R_T will be

$$R_T = R_{S1} + R'_{S1} + R_P. \quad (7)$$

Knowing the total DC resistance, we can calculate the transmission coefficient, the ratio of incident voltage and reflected voltage

$$\Gamma = 2R_T/(R_T + 50). \quad (8)$$

For pulse measurements where the transient part of the pulse is negligible (2 ns) comparing to the steady state part (60 ns–100 ns), we do not take into account parasitic capacitance and inductance from the device and the testing circuits in the transmission coefficient calculation.

Also we can write the expression for voltage seen on the oscilloscope V_O as

$$V_O = V_I \Gamma \frac{R_P}{R_T} \frac{50}{R_{S2} + R'_{S2} + 50}, \quad (9)$$

where V_I is the input voltage. Combining Eqs. (5)–(9), we can calculate $\Delta\overline{T_{eff}}$ from each data point associated with V_O and extract the temperature as a function of time.

The temperature $\overline{T_{eff}}$ extracted from the resistance $R_{H,\Delta T}$ is defined as the effective average temperature. The effective average temperature $\overline{T_{eff}}$ can be considered as the spatial average temperature $\overline{T_V}$ if we assume that temperature is uniformly distributed in the heater strip (section A shown in Fig. 2) so that temperature of each part of the heater has the same contribution to the resistance change. The increased $\overline{T_V}$ is defined by (10) given the temperature as a function of position in the heater

$$\Delta\overline{T_V} = \frac{\int_V \Delta T(x,y,z)dV}{V}. \quad (10)$$

However, lateral heat flow along the length of the heater (vertically from top to bottom as oriented in Fig. 2) causes non-uniform temperature distribution. $\overline{T_{eff}}$ can still be regarded as an approximation of $\overline{T_V}$ if the following two assumptions are valid. First, the temperature is uniform along the width of the heater (horizontal direction as oriented in Fig. 2). Second, the resistance per unit length along the length of the heater strip is constant. A detailed proof is discussed in Section II E.

E. Proof of $\overline{T_{eff}}$ approximates $\overline{T_V}$

Using the first assumption in Section II D, (10) can be reduced to a 1-D integral as

$$\Delta\overline{T_V} = \frac{\int_0^l \Delta T(x)dx}{l}, \quad (11)$$

where x is coordinate along the length of the heater and l is the length of the heater. Thus x is 0 on one end of the heater and l on the other end.

One can also write down the heater resistance $R_{H,\Delta T}$ in a distributed form

$$R_{H,\Delta T} = \int_0^l (r_H(x)(1 + \alpha \Delta T(x)))\, dx, \quad (12)$$

where $r_H(x)$ is the room temperature resistance per unit length of the heater. The heater resistance at room temperature is given by

$$R_H = \int_0^l r_H(x)dx. \quad (13)$$

Substituting (13) into (12), the heater resistance is

$$R_{H,\Delta T} = R_H + \int_0^l (r_H(x)\alpha \Delta T(x))\, dx. \quad (14)$$

Combining (5) and (14), we can write the distributed form of $\Delta\overline{T_{eff}}$ as

$$\Delta\overline{T_{eff}} = \frac{\int_0^l r_H(x)\Delta T(x)dx}{R_H}. \quad (15)$$

Thus effective average temperature $\Delta\overline{T_{eff}}$ is the average temperature weighted by distributed resistance. Using the second assumption, $r_H(x)$ can be written as a constant r_H and $R_H = lr_H$. $\Delta\overline{T_{eff}}$ can be rewritten as

$$\Delta\overline{T_{eff}} = \frac{r_H \int_0^l \Delta T(x)dx}{R_H} = \frac{\int_0^l \Delta T(x)dx}{l}. \quad (16)$$

It is proved from (11) and (16) that $\Delta\overline{T_{eff}} = \Delta\overline{T_V}$ based on the assumptions described above. $\Delta\overline{T_{eff}}$ can be used to approximate $\overline{T_V}$ and the temperature extraction method can be a quick way of thermometry without simulations.

III. RESULTS AND DISCUSSION

A. Preparatory DC measurements

The measured parameters determined prior to the TDT measurements as described above are shown in Table I. Using the arrangement shown in Fig. 4 and Eqs. (1)–(4), we measured $R_{S1} + R'_{S1}$ and $R_{S2} + R'_{S2}$.

Fig. 5 shows the measured device resistance R_D as a function of heater length. The linear fit has an intercept of 8.16 Ω which is the device lead resistance R_L. Since $R_D = R_H + R_L$, we can calculate the ratio of heater resistance R_H to R_D for a 5 μm long heater. We used the ratio instead of the actual measured R_H because R_D may be different from device to device, due to thickness variation. We then calculated R_H for the device under test (with a heater length of 5 μm) using this ratio and its value of R_D.

Fig. 6 shows the TCR measurement results. The uncertainty in the measurement is indicated by the size of data points which are ±2 °C in temperature and ±3 mΩ/□ uncertainty in sheet resistance. A linear fit to the data gives a TCR of

TABLE I. Parameters for extracting temperature.

Parameters	Values
$R_{S1} + R'_{S1}$ (Ω)	2.86 ± 0.02
$R_{S2} + R'_{S1}$ (Ω)	4.17 ± 0.02
R_H (Ω)	12.90 ± 0.1
R_D (Ω)	20.16 ± 0.2
R_H/R_D	0.64 ± 0.01
TCR (ppt/K)	2.2 ± 0.1

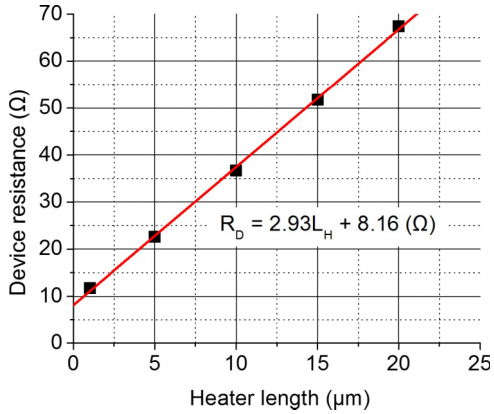

FIG. 5. Device resistance measurements as a function of heater length, where device resistance $R_D = R_H + R_L$.

2.2 ± 0.1 ppt/K. From Ref. 24, the extracted bulk tungsten TCR data are 5.8 ppt/K and electrical resistivity at room temperature is 54.6 nΩ m. This is consistent with Matthiessen's rule,[29] which describes the resistivity as $\rho = \rho_L + \rho_i$, where ρ_L is the temperature dependent term caused by thermal phonons and ρ_i is the temperature independent term caused by electron scattering effects. For thin film metal resistivity, we have

$$\rho = \rho_i + \rho_{RT}(1 + \alpha_b \Delta T), \tag{17}$$

where ρ_{RT} is the bulk resistivity at room temperature and α_b is the bulk TCR. It shows that the measured thin film resistivity ρ is sum of the temperature independent term ρ_i and temperature dependent term $\rho_L = \rho_{RT}(1 + \alpha_b \Delta T)$. We also have

$$\rho = (\rho_i + \rho_{RT})(1 + \alpha \Delta T), \tag{18}$$

where α is the thin film TCR. It shows that ρ is dependent on thin film room temperature resistivity $\rho_i + \rho_{RT}$. From (17) and (18), we can derive thin film TCR as

$$\alpha_b/\alpha = (\rho_{RT} + \rho_i)/\rho_{RT}. \tag{19}$$

For the 55 nm fabricated tungsten thin film, the room temperature electrical resistivity is higher than the bulk value by a factor of 2.64, which is the measured value of $(\rho_{RT} + \rho_i)/\rho_{RT}$ in Equation (19). While the tungsten thin film TCR is lower than the bulk value by a factor of 2.62, which is the measured value of α_b/α in Equation (19). Thus, the measurement values are consistent with the theoretical derivation, as expected. On the other hand, we can also conclude from (19) that thin film TCR is constant as long as bulk TCR remains constant over the entire temperature range of interest.

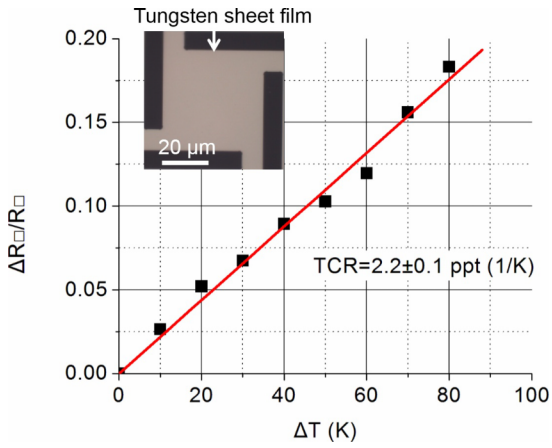

FIG. 6. TCR measurement results. (Inset) van der Pauw structure used to measure sheet resistance for TCR measurements.

B. Pulse measurements

Since contact resistance is strongly dependent on the contact condition between the probes and the pads, we performed pulse measurements immediately after the DC measurement to keep conditions unchanged for both probes. Using the arrangement shown in Fig. 3(a), the TDT measurement was performed on the device under test. Fig. 7(a) shows the input pulse from the pulse generator. The pulse has a maximum voltage of 5 V and a 1 V dc bias. The 1 V dc bias is used to read the resistance change after the pulse is "off" without causing significant heating in the heater. Simulation shows that 1 V bias will generate ΔT of 26 K from room temperature in the heater at steady state, which is less than 4% of the target temperature (1000 K) for the heater. The rise and fall time, defined as the time for the voltage to change between 90% and 10% of the total voltage difference, are both 2 ns. The pulse maximum voltage was fixed and the pulse width varied to bring the heater to different temperatures.

Fig. 7(b) shows the transient voltage as observed on the oscilloscope for 60 ns, 80 ns, and 100 ns wide pulses. The solid lines are simulated results while the noisy lines are measured. The calibrated measured voltage and simulated voltage are in good agreement with each other and the mismatch is smaller than 1.9%. The narrow peaks and small bumps observed in the voltage curves after the pulse is off are possibly due to the reflection of inductive discontinuity in the measurement circuits, where the inductive discontinuity is caused by the parasitic inductance of the scope and the reflection is due to the impedance mismatch between cables and connectors. Fig. 7(c) shows the simulated and measured lumped heater resistance as a function of time for different pulse widths. These also are in good agreement on the ramp up region and part of the ramping down region (with mismatch smaller than 1.2%). The larger mismatch of 26.9% that lasts 20 ns after the pulse is turned "off" is due to the reflection in the voltage.

Fig. 8(a) shows the modeled temperature as a function of position along the length of the heater (vertically from top to bottom as oriented in Fig. 2) right before the pulses was turned off. Due to the lateral heat flow in the heater, the temperature distribution along the length of the heater is not uniform. Different parts of the heater contribute differently to the measured heater resistance change. However in Fig. 8(b), the temperature distribution is much more uniform along the width of the heater. This is due to limited heat flow in the width direction.

Simulated $\overline{T_V}$ and $\overline{T_{eff}}$ (extracted from simulated resistance transient shown in Fig. 7(c)) are plotted versus $\overline{T_V}$ for a 5 V 100 ns pulse as shown in Fig. 8(c). The good consistency (with mismatch smaller than 0.8%) between simulated $\overline{T_V}$ and $\overline{T_{eff}}$ confirms that the distribution is uniform enough for the first

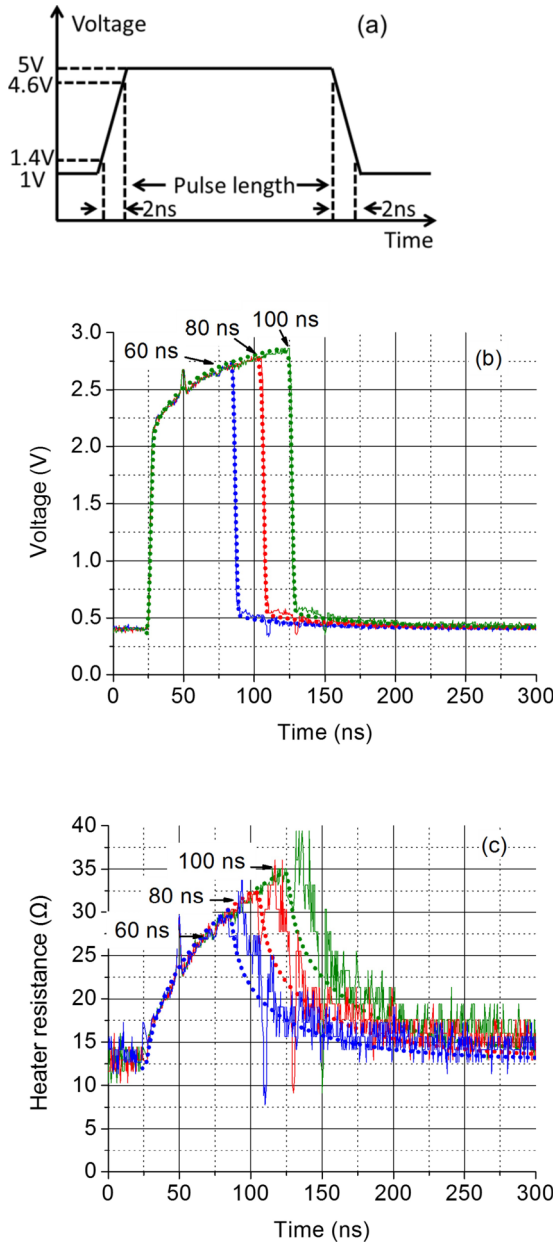

FIG. 7. (a) Input pulses with fixed voltage level and varied pulse length, (b) simulated (dotted lines) and experimental (solid lines) voltage transmitted to the scope as a function of time for different pulse widths, and (c) simulated (dotted lines) and experimental (solid lines) lumped heater resistance change as a function of temperature.

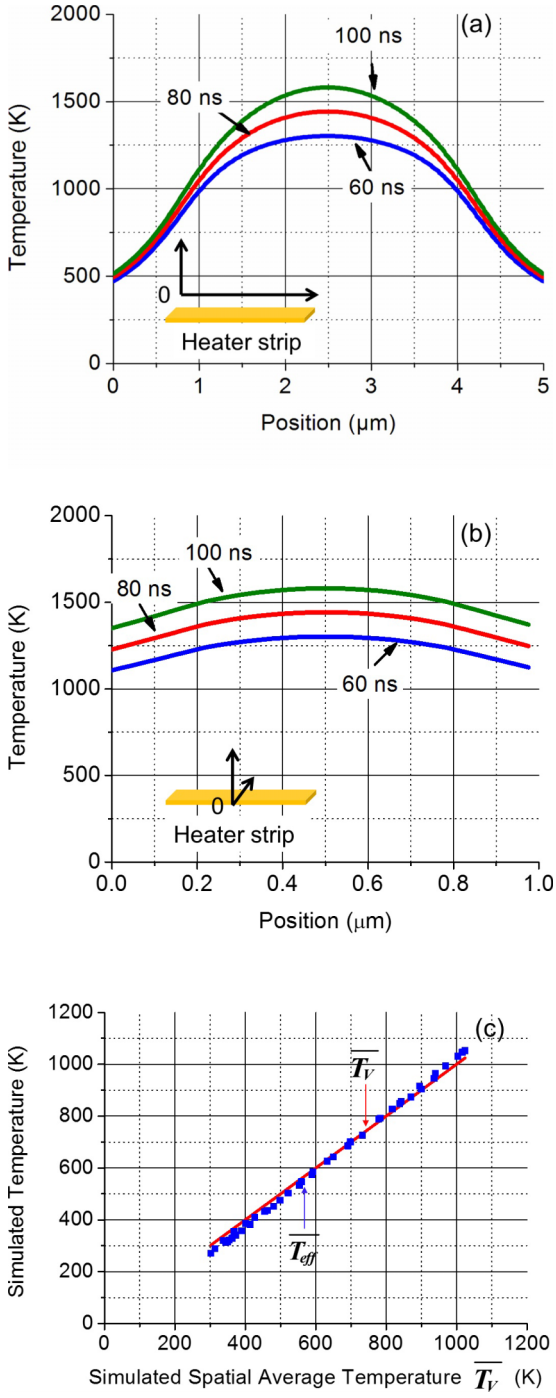

FIG. 8. Simulated temperature profile (a) along the length of the heater and (b) along the width of the heater at 60 ns, 80 ns, and 100 ns and (c) $\overline{T_{eff}}$ and $\overline{T_V}$ plotted versus $\overline{T_V}$ for a 5 V 100 ns pulse.

assumption in Section II D to be valid. Since the cross section area of the heater strip is designed to be the same along the length of the heater, the second assumption is also valid that the resistance per unit length of heater is constant. Thus, $\overline{T_{eff}}$ should be a good approximation of $\overline{T_V}$.

Using Eqs. (5)–(9) and parameters (series resistances, heater strip resistance, and TCR of tungsten) determined in the DC measurement, $\overline{T_{eff}}$ was extracted from the measured heater resistance transients in Fig. 7(c). In Fig. 9, the dotted lines are simulated $\overline{T_V}$ and the solid lines are $\overline{T_{eff}}$ extracted from measurement and they are in good agreement.

Fig. 9 shows that the maximum $\overline{T_V}$ of 60 ns, 80 ns, and 100 ns wide pulses are 880 K, 960 K, and 1050 K, respectively. In the central 1 μm region, the maximum temperatures are 1309 ± 9 K, 1457 ± 14 K, and 1664 ± 20 K. In this region, the temperature distribution is relatively uniform and one is able to heat uniformly and predictably in this region. For the 100 ns wide pulse, the heating rate in the center of heater is 1.67×10^{10} K/s.

Despite the fact that there is 26.9% mismatch during the 20 ns immediately after the pulse is turned "off," we were still able to measure an effective RC time constant, which is defined as the time needed for the heater temperature to cool from 100% to 37% of its maximum temperature. The values we found were 28 ns for the 60 ns wide pulse and 38 ns for the

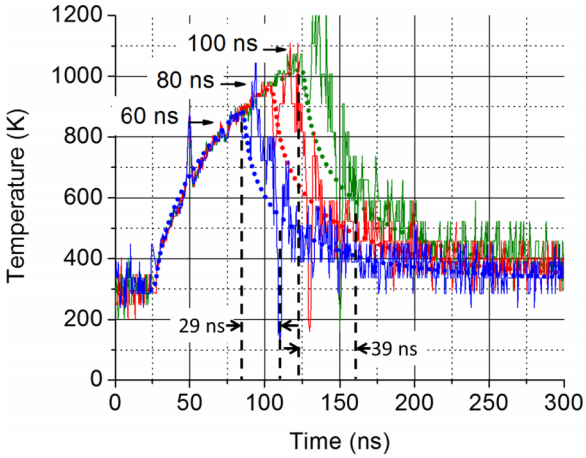

FIG. 9. (Dotted lines) Simulated $\overline{T_V}$ and (solid lines) extracted $\overline{T_{eff}}$ according to lumped heater resistance change in Fig. 7(c) and TCR of tungsten.

100 ns wide pulse. Since this is a distributed thermal system that can be approximated as a system with multiple thermal time constants, the above temperature transient reflects the *shortest* time constant of the system. To reach true steady state, requires about 1 μs, the longest time constant of the system. By using short pulses we avoid activating these slower cooing thermal reservoirs and can operate at high speed. It should be noted that the increase of the observed time constant with increasing pulse length indicates increasing activation of the slower cooling reservoir, consistent with our understanding of the multi-time constant system response. At higher temperatures the sapphire thermal conductivity is lower and the heat capacity is higher, typically at 1500 K, k_{th} = 12 W/(m K), and C_p = 1290 J/(kg K); therefore, the time constant is larger.[26,27] Since the temperature distribution along the length of the heater is not uniform, the thermal RC time constants in the center of the heater will be higher than the lumped values.

In another set of pulse measurements, the pulse width was fixed and the input voltage set to 5 V, 6 V, and 7 V. Fig. 10(a) shows the fit for simulated and measured oscilloscope voltage. Fig. 10(b) shows the modeled temperature distributions along the length of the heater at 100 ns. As can be seen, the higher the temperature the less uniform the temperature distribution.

For the temperature simulation with a 7 V input voltage, the temperature profile along the length of the heater shows an abrupt change in the center and the central temperature is slightly higher than the melting temperature. We attribute this to the latent heat of fusion of tungsten. When heater temperature reaches the melting temperature of tungsten, the heat capacity of tungsten becomes enormous (higher than 5 kJ/(kg K)) and this slows the heating rate in the material as it melts. Our simulations include the effects of the latent heat of fusion as the material melts. The melting temperature is set to be 3695 K, latent heat of fusion is set to be 260 kJ/kg,[30] and the transition interval temperature range is 50 K. No SEM measurements were made to inspect the structure after the pulsing measurement to confirm melting, but the electrical response is consistent with the large body of work on the subject.

In Table II, simulated and extracted temperatures for different pulse inputs in terms of voltage and time are compared. The consistency between maximum simulated $\overline{T_V}$

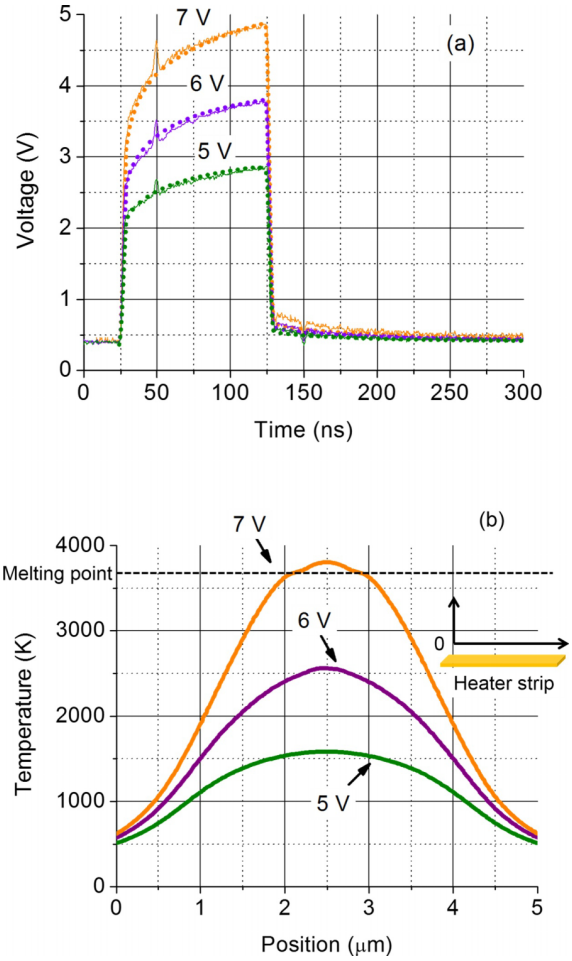

FIG. 10. (a) Simulated (dotted lines) and experimental (solid lines) scope voltage as a function of time for different input voltages. (b) Simulated temperature as a function of position at 100 ns for different input voltages.

and maximum extracted $\overline{T_{eff}}$ decreases when the temperature is higher. We attribute this growing difference in extracted and simulated maximum temperatures to the simulated $\overline{T_V}$ being less accurate in predicting the extracted temperature when the distribution is less uniform in the width direction. We have a very good consistency between simulation and extracted temperatures with a mismatch smaller than 5.5% when maximum extracted $\overline{T_{eff}}$ are smaller than 1535 K. For the highest temperature, part of the tungsten was melted and due to the latent heat of fusion, the non-uniformity is even stronger. The mismatch is 13.1%, suggesting that the temperature prediction has limited accuracy at this operating point.

C. Durability measurement

Fig. 11 shows the device resistance as a function of pulse number. This measurement provides a sense of the durability

TABLE II. Comparison for simulation and extracted temperature.

Input voltage (V)	5	5	5	6	7
Pulse width (ns)	60	80	100	100	100
Max extracted $\overline{T_{eff}}$ (K)	884	981	1074	1535	2290
Max simulated $\overline{T_V}$ (K)	886	960	1024	1450	1990
Mismatch (%)	0.2	2.1	4.7	5.5	13.1

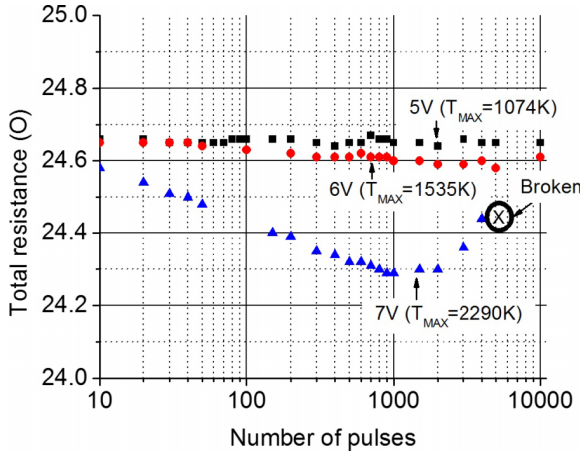

FIG. 11. Cycling test results at different pulse height. Pulse width and pulse edge are fixed at 100 ns and 2 ns. The device was broken after 5000 pulses at 7 V (maximum extracted $\overline{T_{eff}}$ is 2290 K).

of the heater. The heater was pulsed using a fixed pulse width of 100 ns with 2 ns rise and fall time and various input voltages. The maximum simulated $\overline{T_V}$ and extracted $\overline{T_{eff}}$ are shown in Table II and temperature distributions at 100 ns are shown in Fig. 10(b). At 5 V, the resistance is 24.654 ± 0.007 Ω through all 10 000 pulses and is very stable, presumably because of the low maximum temperature. At 6 V, the resistance slightly decreases from 24.65 Ω to 24.58 Ω with more pulses cycling the heater. We attribute this due to the annealing of the tungsten at higher temperature, possibly causing grain growth in the tungsten. At 7 V, the resistance decreases significantly and continuously from 24.58 Ω to 24.30 Ω because the $\overline{T_V}$ is higher and the temperature at the central region of heater is above the melting point of tungsten. The heater was destroyed after 5000 pulses at 7 V. When we attempted to increase the pulse maximum voltage to 8 V, the heater failed immediately. With this heater design a 5 V 100 ns pulse allows our device to maintain the heater resistance over time and at a maximum central temperature of 1664 K. The heater also shows some durability for a limited number of pulses at ultra-high center temperatures of 3800 K (7 V pulses).

IV. CONCLUSION

Geometry and fabrication process of a micro-heater using thin film tungsten on a sapphire substrate for high temperature high speed heating are described. This heater design is able to reach a maximum central temperature of 1664 K at a rate of 1.67×10^{10} K/s. The heater is also able to quench quickly with a thermal RC time constant of less than 40 ns. TDT was used to measure the heater temperature as a function of time and the measurement results can be accurately predicted and verified by a 3-D COMSOL model. The maximum $\overline{T_V}$ mismatch between measurements and simulations is less than 0.2% in the best case with a lower temperature and 13.1% in the worst case with a higher temperature. The heater also shows very good stability at a center temperature of 1664 K and can even be operated up to 2550 K. This heater has great potential for use as an external heater for phase change switches and perhaps also in additional applications such as calorimetery.

ACKNOWLEDGMENTS

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Transient Thermometry and HRTEM Analysis of RRAM Thermal Dynamics during Switching and Failure

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***Abstract*— We investigate RRAM thermal dynamics during resistive switching and endurance failure by using transient thermometry and HRTEM analysis. The filament size was estimated to ~1 nm with 7-15 nm crystalline region, having experienced local temperatures of > 1600 K at the filament core and > 850 K in the heat affected zone. The devices that underwent cold switching show no change in the $HfAlO_x$ microstructure, post-programming. However, such devices show preferential templated growth of $HfAlO_x$ crystallite, extending from the polycrystalline Hf layer after 10^7 switching cycles, eventually culminating in a RESET failure.**

Keywords; RRAM, thermometry, HRTEM, filamentary

I. Introduction

Resistive Random Access Memory (RRAM) has emerged as an attractive candidate for storage class memory [1]. Since resistive switching event is directly connected to the characteristics of conductive filaments, estimating the filament size is of critical and has been the active research topic. Knowing the filament size, one can have a deeper insight into the switching mechanism and engineer superior devices. There have been reported some experimental results representing the 100 nm range filament size [2]. On the other hand, device scaling suggests the filament sizes are below 10 nm[3]. The important consequence of the filament size is the filament temperature generated during switching [4], [5]. The filament temperature estimation has relied on simulations with a number of assumptions about the conductivity, size, and geometry of the filament [6], [7].

In this work, we combine novel transient device thermometry and high-resolution transmission electron microscopy (HRTEM) to estimate the conductive filament size, and understand the role of nanoscale temperature excursions. Also, the temperature gradients and phase transformation in the switching and endurance failed RRAM cells have been investigated.

II. Filament Properties from Transient Thermometry

The RRAM devices considered in this study are of cross-bar type (Fig. 1(a)) with a 85 nm MIM stack consisting of TiN/a-$HfAlO_x$/Hf/TiN. The device is encapsulated by SiO_2/SiN passivation. The device undergoes the forming and switching processes as shown in Fig. 1(b).

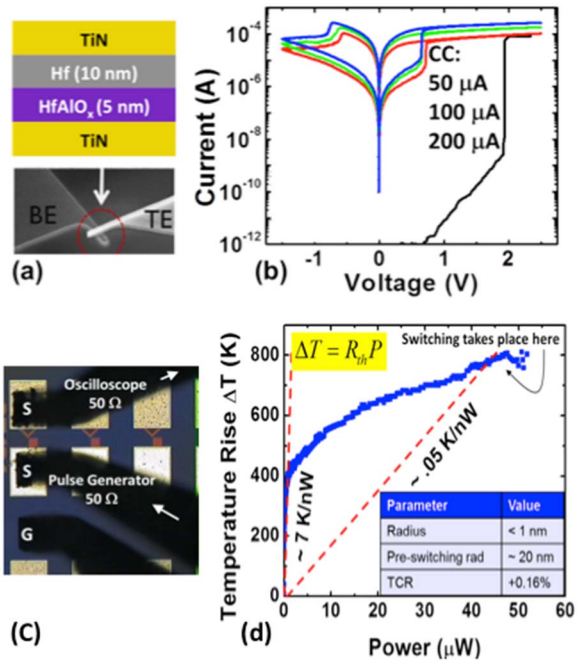

Fig. 1. (a) Cross-sectional view of TiN/Hf/$HfAlO_x$/TiN device stack (b) *I-V* characteristics showing forming (black) and switching. (c) High speed transient thermometry setup. (d) ΔT vs. Power showing a high initial slope corresponding to small size filament. At high power adjacent region starts conducting due to temperature rise (ΔT).

A nearly linear low resistance state (LRS, 50 µA compliance current (CC)), is identified with a conductive filament (CF) [8], which undergoes temperature excursion during biasing. In order to isolate the effect of temperature, we use transient thermometry [7], [9]. For this, we measure the pulsed *I-V* characteristics of the device with time domain

transmissometry [9] using 80 ps pulses. Fig. 1(c) shows the pulsed thermometry setup and sample. This ensures that the self-heating in the device is minimal. The pulsed *I-V* characteristics are then used as a lookup table to ascertain the temperature at each LRS point of the *I-V*, as discussed in our previous work [7], [9]. The observed effective temperature coefficient of resistance is α = 0.16 %/K, indicating that the composite of the filament and its matrix becomes more conductive with temperature. Filament size is estimated from the plot of temperature rise *vs.* dissipated power, *P*, (Fig. 1(d)) which shows that temperature excursions (ΔT) of > 800 K can be reached during DC switching when *P* ~40 µW (as also simulated in [5]). The slope of this plot is thermal resistance, R_{th} (= $\Delta T/P$) and is dependent on the filament thermal properties/geometry and can be simulated (Fig. 2(a)). Thus a small filament with a smaller cross-sectional area dissipates heat less efficiently compared to a large conducting volume. The slope (R_{th}) is a bulk equivalent thermal resistance as seen by the conducting area. This 'conducting area' corresponds to the filament at low powers and corresponds to the aggregate of the filament and the heated zone at high powers. A change in slope of ΔT *vs* *P* (Fig. 1(c)) implies a change in the radius of the heated-zone.

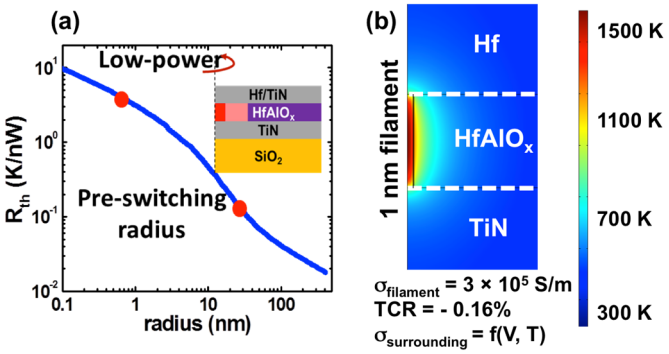

Fig. 2. (a) Simulated R_{th} versus radius of heat generating zone. (b) Simulated temperature map of the device assuming the measured filament geometry, TCR and conductivity at pre-switching bias of ~ 0.5 V.

At low-power the slope is 7 K/nW, consistent with a CF radius of 1 nm having a room-temperature conductivity of 3×10^5 S/m. However, the conducting region grows to 20 nm at 0.8 V (corresponding to low slope of ΔT *vs* *P*, R_{th} ~ 0.05 K/nW). This saturation in the ΔT results from current and heat spreading (i.e. power density reduction) due to increases in the electrical conductivity of the surrounding heated $HfAlO_x$. By using the filament properties obtained through thermometry, and the temperature dependent *I-V* characteristics of the matrix material, we obtain a temperature map of the device, as shown in Fig. 2(b). Fig. 3 is the 1-D profile of the modeled temperature profile in the middle of the $HfAlO_x$ layer, suggesting that the peak filament temperature is > 1600 K at the center.

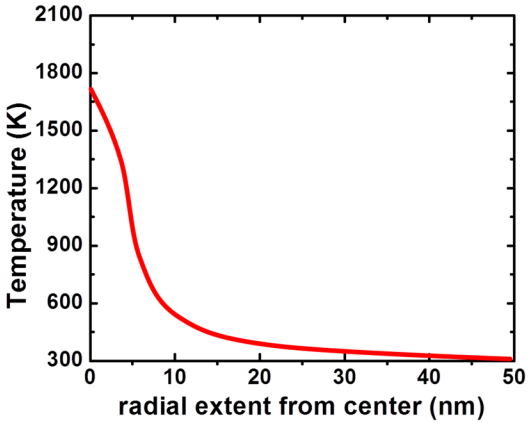

Fig. 3. 1-D profile showing extension of hot zone.

III. Microstructure of Programmed Devices

In order to investigate the microstructural change and understand the role of temperature in switching and endurance cycling, we conducted TEM characterization of the stacks before and after the programming. The TEM analysis was performed by using a C_s-corrected FEI Titan operated at 300 keV. The TEM specimens were prepared by a FEI Nova 600 dual-beam focused ion beam (FIB). The thickness of the specimen was ~80 nm after 5 keV ion beam polishing. The entire active of the device (65×65 nm^2) was captured within the TEM specimen with a careful precision ion milling. To image all the possible switching-induced structural changes in the device, multiple images at the same location were collected with different objective lens strength (through focus imaging series).

Fig. 4 shows the cross-sectional HRTEM micrographs showing the microstructure of the as-fabricated device. It is seen that the Hf and TiN layers are polycrystalline. The lightest contrast around the device stack is SiO_2 passivation. The $HfAlO_x$ functional layer is completely amorphous. This has been confirmed by examining a much larger area of the device (1×1 µm^2, not shown here).

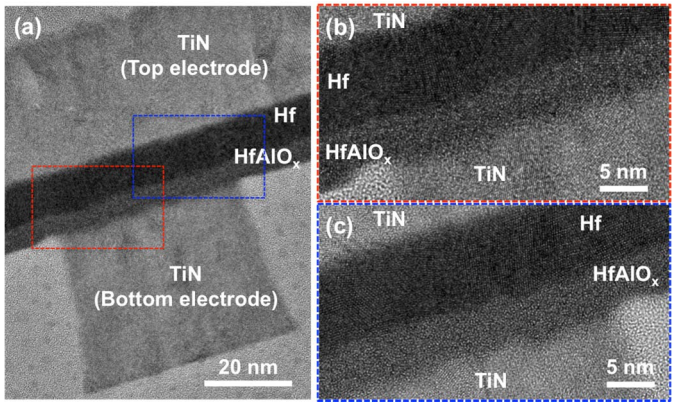

Fig. 4. HRTEM image of an unformed device showing completely amorphous $HfAlO_x$ microstructure

Similar TEM analysis has been conducted on devices that were programmed with the current compliances set at 10 µA, 50 µA, 200 µA which are set by on-chip transistors as ballasts. Fig. 5 shows a single crystallite delineated by dashed lines (tetragonal $HfAlO_x$ with a lattice parameter of d_{101}=~0.30 nm) embedded in an amorphous $HfAlO_x$ matrix. The crystallite size is ~7 nm (diameter) at 10 µA CC and ~15 nm (diameter) in both the 50 µA and the 200 µA CC. We interpret the local crystallization is an indication of switching-induced phase change of the amorphous $HfAlO_x$ caused by local heating of the oxide around the conducting filament. It is important to note that the crystalline $HfAlO_x$ is not electrically conductive and the crystallites are not the filament itself. Instead, they are merely microstructural change indicative of appreciable, local Joule heating.

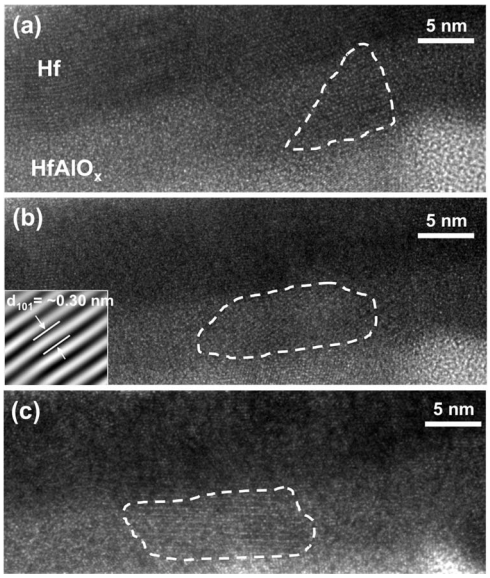

Fig. 5. Crystallization of $HfAlO_x$, as observed in devices subjected to CC of (a) 10 µA, (b) 50 µA and (c) 200 µA testing. The lattice fringes correspond to d_{101} ~ 0.30 nm $HfAlO_x$. Inset in (b) is an inverse Fast Fourier Transform (FFT) of the crystalline area.

The $HfAlO_x$ crystallization temperature was determined by combining rapid thermal annealing (RTA) and through focus HRTEM analysis. RTA conducted in N_2 environment for 2 s at 820 K, 870 K, 920 K and 970 K. Fig.6 shows the TEM micrographs of RTA specimens, representing no change in the 820 K specimen, with 50 % crystallization in 870 K and 70 % in 970 K. The crystallites are outlined by white dashed lines and the observed d-spacing was again ~0.30 nm in all cases. And it appears that the crystallites in $HfAlO_x$ grow from the Hf layer with the same lattice fringe orientation. Fig. 7 shows degree of crystallization as function of different RTA temperatures indicating a clear transition occurring at 850 K. Thus, we set the crystallization zone as the region exposed to temperatures > 850 K. Assuming ~1 nm filament extracted from thermometry, our electro-thermal simulation (COMSOL package) reveals that the hot zone (~14 nm) corresponding to temperatures > 850 K (Fig. 3) is consistent with the observed crystallite sizes (~15 nm). *I-V* measurements for annealed devices reveal the device resistivity does not change, which confirms the crystallite itself is not the conductive filament, but rather is caused by localized heating.

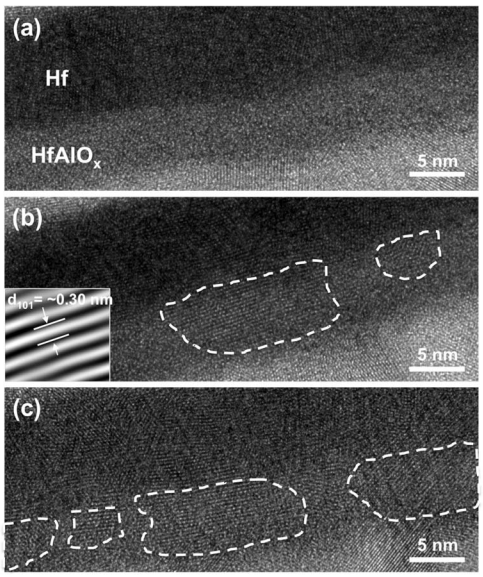

Fig. 6. HRTEM images showing RTA on pristine devices exposed to (a) 820 K, (b) 870 K, (c) 970 K. Inset in (b) is an inverse FFT of the crystalline area.

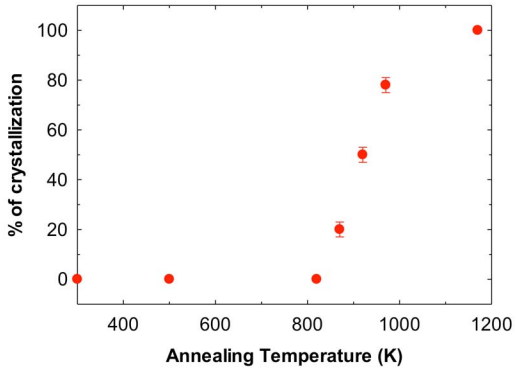

Fig. 7. Degree of crystallization as a function of different RTA temperatures showing a clear transition occurring at temperatures > 850 K.

IV. Microstructure of Programmed Devices

In order to understand the failure mechanisms in RRAM cells, we use the thermometry and TEM analysis on devices that have undergone endurance cycling. Fig. 8(a) shows endurance cycling of $HfAlO_x$ devices, subjected to 10^7 cycles of SET and RESET pulses with a CC of 50 µA. The red curve corresponds to a median device in the OFF state (HRS) and the blue curve corresponds to a median device in the ON state (LRS); the gray traces represent the entire set of devices. After ~10^7 cycles, the resistance of these devices reduces such that the HRS-LRS window collapses and the devices undergo RESET failure. The device undergoing pulse switching experiences lower temperature excursions [10] and show no post-forming microstructural change (i.e. $HfAlO_x$ remains amorphous).

However, it is seen that the devices undergoing the RESET failure show local crystallization does not extend through the entire $HfAlO_x$ layer thickness. This could indicate an asymmetric temperature distribution along the filament due to asymmetric heat flow during cold switching [6], [10]. Moreover, the heat dissipation is mainly through the bottom electrode to the thermal ground. This introduces additional asymmetry in the temperature distribution, making the top electrode interface hotter, eventually leading to crystallization, as seen in Fig. 8(b). The lattice fringes in $HfAlO_x$ are continuous across the Hf/$HfAlO_x$ boundary implying that the crystallite growth initiates at the interface. The observed crystallite in the RESET failed device could represent an atomic relaxation and consequence degradation of oxygen vacancy mobility, which eventually causes the RESET failure [11].

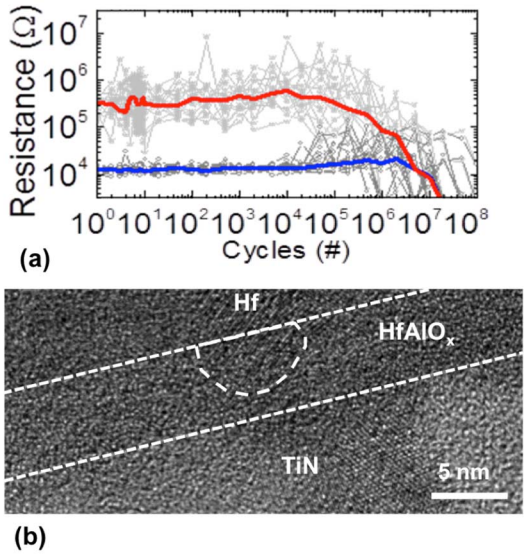

Fig. 8. (a) Endurance cycling of $HfAlO_x$ at 1.75 V with CC of 50 µA suing pulse widths of 100 ns (b) HRTEM image of endurance cycled $HfAlO_x$ device. Crystallite extends from top electrode after pulse switching till endurance failure (RESET failure). V_{SET} = -2.5 V, V_{RESET}= -2V at pulse width of 100 ns.

V. Conclusion

Using transient thermometry and HRTEM analysis, we estimate the filament size ~1 nm with 7-15 nm crystalline region embedded in amorphous matrix, having experienced local temperatures of > 1600 K at the filament core and > 850 K in the heat affected zone. This is makes the HRTEM analysis, thermometry and finite element simulation self-consistent and a powerful tool in understanding the temperature excursions during switching and failure. The devices that underwent cold switching show no change in the $HfAlO_x$ microstructure, post-forming. However, such devices show preferential templated growth of $HfAlO_x$ crystallite, extending from the polycrystalline Hf layer after 10^7 switching cycles, eventually culminating in a RESET failure.

Acknowledgment

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Low-Power, High-Performance S-NDR Oscillators for Stereo (3D) Vision using Directly-Coupled Oscillator Networks

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Introduction: Directly coupled oscillator networks offer tremendous potential for a wide range of computing applications including oscillatory neural networks (ONNs) [1], directly-coupled non-linear networks [2,3] and phase-based logic [4], exploiting the oscillator phase as the associative network's state variable [1-5], thus offering the massive parallelism needed for efficient pattern recognition. However, to date the requisite oscillators and network co-design needed for approximate computation has not been explored. This work highlights how stack-engineering can enable the use of S-type NDR (negative differential resistance) devices as compact oscillators for implementing stereo (3D) vision using directly-coupled oscillator networks. We explore a novel composite of $GeTe_6$ (chalcogenide) and $HfTaO_x$ (oxide) that can be engineered as a 1T1R integrated oscillator with best-in class low-power (< 30 μW), low-leakage (< 1 nA), low-voltage (~ 1 V), improved endurance (> 10^{12} cycles) with frequency tunability. Using a Van der Pol formalism to model oscillator dynamics, we demonstrate a full loopy-belief stereo vision system simulation that utilizes unique oscillator and array characteristics to accelerate graph-based inferencing [6] through co-design, offering 16x improvement in performance, consuming 100x lower energy compared to conventional FPGA implementation from our previous work [17] & others [18].

Engineering Leakage: Chalcogenide devices show reversible threshold switching and oscillations but eventually fail due to crystallization of a conducting phase [7]. Moreover they show large leakage current due to their narrow bandgap and thermal carrier generation [8]. Oxides show much lower leakage due to their higher bandgap, but suffer from electroforming as a 'failure' mechanism [15]. In this study we make composite structures using amorphous-$GeTe_6$, a threshold switching chalcogenide; and amorphous-$HfTaO_x$, a wide-bandgap (~5 eV) threshold switching oxide in varying volume fractions. We co-sputter different compositions of the two constituents ranging from 0% to 100% $HfTaO_x$ in a $GeTe_6$ matrix, while keeping the stack thickness constant at 50 nm (Fig. 1 (a)). The structure is a 700 nm × 700 nm MIM stack ballasted with a PMOS transistor akin to our earlier demonstration [9]. The S-NDR *I-V* characteristics of $HfTaO_x$ and $GeTe_6$ are shown as an overlay in Fig. 1(b) with threshold voltage as a function of composition in Fig. 1(c). Fig. 1(d) shows an OFF state down to ~10 pA, indicating that the leakage through percolation paths steadily decreases with increasing wide-bandgap $HfTaO_x$ percentage and the Schottky-contact with the electrode. This affects the power consumed by these oscillators which is a time averaged product of voltage and current.

ON-state Power: The second source of power consumption in these oscillators is the ON-state. Only oscillators operating at low currents in the ON-state can limit power dissipated in these dense oscillator arrays but they have lower frequencies [16]. To balance this, one seeks to maximize the ratio of holding current, I_h (the minimum ON-state current) to threshold current, I_{th}, so that a greater control over power and frequency can be achieved. The actual oscillator current will then be set by the load line. Fig. 2 shows this window widen for increasing oxide content.

Engineering Endurance: We find that, in several cases, the frequency of oscillations appears to drift with time and is accompanied by a change in the peak current overshoot as well (Fig. 3). This is typically attributed to localized crystallization in the chalcogenide [7] or partial oxygen vacancy agglomeration in oxides [6]. Fig. 4 plots the endurance cycles as a function of material volume fraction, suggesting that a composite prevents crystallization of $GeTe_6$ due to the presence of oxide materials; and vice versa (endurance of > 10^{12} cycles). As the oscillator is inherently low-power, parallel-locking improves the SNR by a power of √N (where N is the # of parallel oscillators), for a preset power envelope. Fig. 5 shows 10 parallel-locked oscillators with increased uniformity of threshold and holding currents, I_{th} and I_h.

Frequency Tuning: We use a PMOS ballast in series with the device (as shown in Fig. 6) to achieve frequency tuning from 12 MHz to 340 MHz as shown in Fig. 7, which is expected to further improve in deeply-scaled CMOS implementations. Moreover, the devices are scaling invariant. Such high frequency operation lends itself naturally to a fast response in networks [9].

Directly-Coupled Network for Stereo Vision: Stereo vision creates an image that serves to provide the depth map of the objects to guide artificial intelligence for classification. Use of a map-based graphical processing scheme requires massive parallelism for efficient implementation [18]. Our previous work on one such graphical software implementation [17] concluded that most of the computation (message generation and passing) is impeded because of raster movement of messages. As shown in Fig. 8, we create the same system using an oscillator network, in which a disparity image is first created as the color difference between left and right images. It is then encoded onto the gate voltage of each 1T1R oscillator (mapping 0 – 255 over a V_G of 0 - 1 V in Fig. 8). Thus, images with larger color difference (objects closer to the camera) will translate to a higher V_G and thus, a higher frequency. Thus, all of the nodes which are a part of the object that is closer to the camera operate at a higher frequency and are locked to the same 180° phase; objects far away operate at a lower frequency, and the edges of these objects too, lock to a 180°, as previously shown [11] to complete a stereo map (Fig. 9, Middlebury benchmark). This phase locking provides frequency stability and prevents drift. Because of variable phase locking, the edges automatically lock at disparate phases. To design large system implementation [16], we develop a data-driven Van der Pol model [16] (Fig. 6) for the array simulation. The presence of an inductor-like circuit element relates filament size to the frequency, which depends on the current [11].

Co-Design: The data cost (depth) is controlled by the mapping of pixel values on to frequency (V_G), and thus, fine grain tunability helps achieve higher resolution (0 – 255 levels). Similarly, coupling capacitance (C_C) controls smoothness cost (edge transitions) and only selecting appropriate C_C (10 – 50 fF) can one achieve stereo vision for a frequency of 1 GHz; a lower value results in poorer coupling and insufficient stabilization of edges. Low-leakage and ON-state power engineered here enables large arrays that overcome aliasing due to block memory-access in large images [18].

Conclusion: We have successfully demonstrated, a best in class low-power, high-performance S-NDR oscillator (benchmarked in Table I) through novel & unique material-engineering of leakage, endurance and by improving SNR through parallel-locking. These oscillators were then connected in form of a dense array that utilized unique array properties to simulate a full stereo-vision system. The system was found to consume 100x lower energy while being 16x better in performance (Table II), when compared to a conventional implementation purely based on computation.

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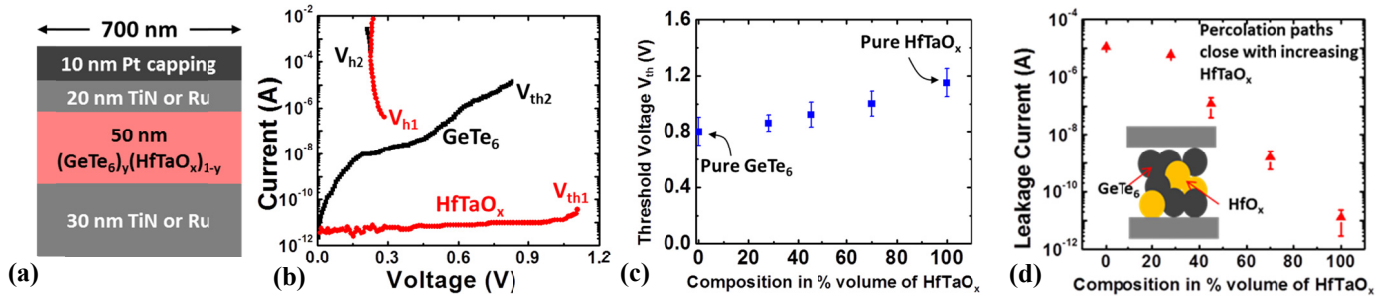


Fig. 1: Material MIM stack, (b) I-V characteristics of devices made with $GeTe_6$ (black) and $HfTaO_x$ (red). (c) Change in the threshold voltage with change in composition. (d) Reduction in leakage with closing of percolation paths by introduction of wide-bandgap oxide.

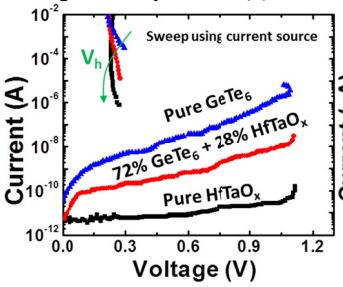


Fig. 2: DC holding currents for three compositions.

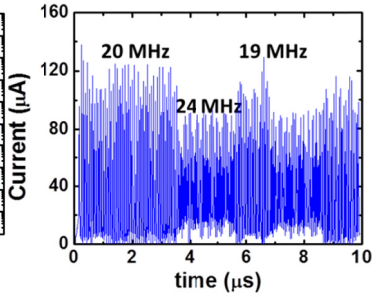


Fig. 3: Variability in some compositions of $GeTe_6$ and $HfTaO_x$.

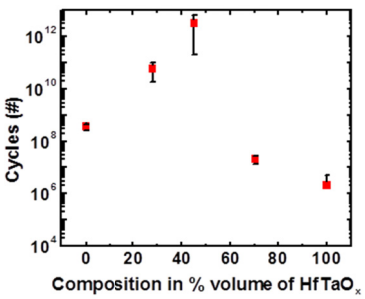


Fig. 4: Endurance improvement with increasing $HfTaO_x$ fraction till 48% due to reduction in ON-state current, followed by degradation due to large *dV/dt*.

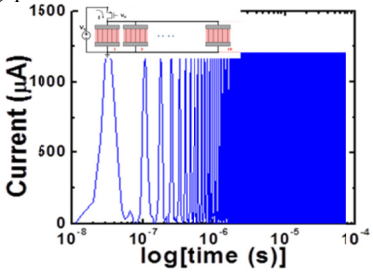
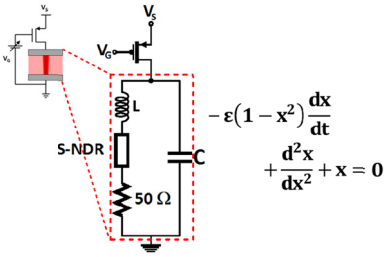


Fig. 5: Reduced jitter and improved amplitude noise due to parallel connection. Time axis in log scale (the frequency does not increase).



$$-\varepsilon\left(1-x^2\right)\frac{dx}{dt}+\frac{d^2x}{dx^2}+x=0$$

Fig. 6: Van der Pol model schematic.

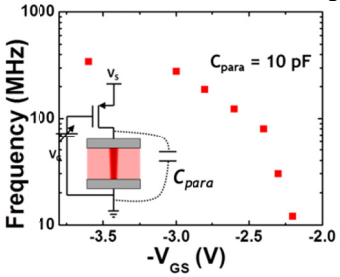


Fig. 7: Frequency tunability by changing V_G.

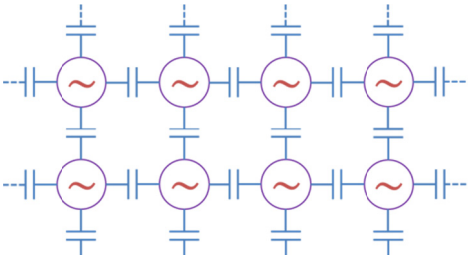


Fig. 8: Coupled oscillator network array.

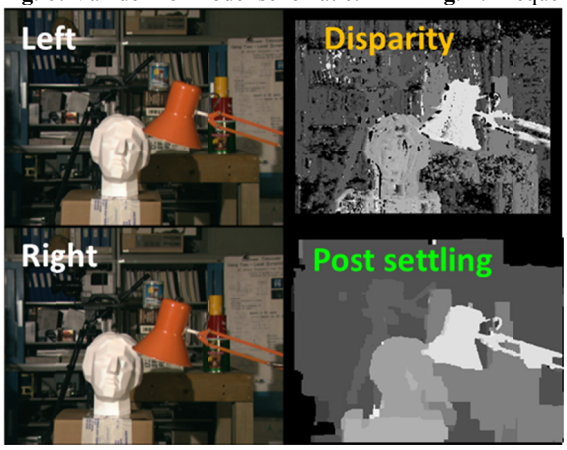


Fig. 9: Left and right images used for create disparity image (by taking the difference), which is fed into oscillator V_G in an array. Bottom right shows a stereo map post-settling. For co-design, 0-255 pixel levels map on to 0 – 1 V; C_C of 10-50 fF can be used for stable network response; Middlebury benchmark used.

Table I: Oscillator	**This Work**	TaO_x [6]	VO_2 [9]	Phase Change [4]
Power (μW)	**< 50**	< 100	2000	< 700
V_{th}, V_h (V)	**1, 0.25**	1, 0.4	8, 5	1.25, 0.75
Area (μm^2)	**0.5**	0.5	24	-
Max. Freq. (MHz)	**350**	500	0.1	< 10
Lat/Vert	**Vert.**	Vert.	Lat.	Vert.
CMOS Comp.	**Y**	Y	N	Y

Table II: Oscillator Network based inference	**This Work**	Previous software implementation (TRWS) [17]
Pixel Misprediction	**22 %**	8 %
Compute speed-up	**16x**	1x
Energy reduction	**100x**	1x

Fig. 10: Benchmarking of oscillator and network.

12.5 THz F_{co} GeTe Inline Phase-Change Switch Technology for Reconfigurable RF and Switching Applications

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***Abstract*—Improvements to the GeTe inline phase-change switch (IPCS) technology have resulted in a record-performing radio-frequency (RF) switch. An ON-state resistance of 0.9 Ω (0.027 Ω·mm) with an OFF-state capacitance and resistance of 14.1 fF and 30 kΩ, respectively, were measured, resulting in a calculated switch cutoff frequency (F_{co}) of 12.5 THz. This represents the highest reported F_{co} achieved with chalcogenide switches to date. The threshold voltage (V_{th}) for these devices was measured at 3V and the measured third-order intercept point (TOI) was 72 dBm. Single-pole, single-throw (SPST) switches were fabricated, with a measured insertion loss less than 0.15 dB in the ON-state, and 15dB isolation in the OFF-state at 18 GHz. Single-pole, double-throw (SPDT) switches were fabricated using a complete backside process with through-substrate vias, with a measured insertion loss 0.25 dB, and 35dB isolation.**

***Index Terms*—germanium telluride (GeTe), inline phase-change switch (IPCS), TOI, IP3, RF switch, SPDT, chalcogenide**

I. Introduction

PHASE-CHANGE materials (PCMs) have been used in optical data storage, such as rewritable CDs, based on Ovshinsky's discovery of the change in optical properties with change in structure in phase-change chalcogenides [1]. More recently, they have been used in digital non-volatile memory devices, taking advantage of the electrical resistance change to improve memory density and switching speed over flash memory devices [2]-[4].

The first demonstration of a functional chalcogenide RF inline phase-change switch (IPCS) was recently reported by El-Hinnawy *et al.* [5]. This device employed an initial design intended to demonstrate the ability to quench chalcogenide PCM in the amorphous state utilizing an integrated, electrically isolated thin-film heater in a horizontal configuration. While only intended to demonstrate the concept for functionality, this design nonetheless achieved an F_{co} (defined as $1/(2\cdot\pi\cdot R_{on}\cdot C_{off})$) of 1.0 THz, which outperforms FETs in frequency performance [6]. By altering device geometry to optimize the complex electro-thermal actuation mechanism, significant performance improvements have since been realized and fabricated into state-of-the art RF circuits.

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II. Device Fabrication

Operation of digital PCM devices has been extensively documented [2]-[4], with some via-style phase-change switches being used for RF applications [7]. Operation of IPCS devices has also been described elsewhere [5], [8], with switch geometry variations being reported as well [9], [10]. A schematic cross-section is shown in Fig. 1(a). Fabrication begins with a dielectric material (substrate insulator) being thermally grown on the surface of the substrate. A SiC substrate is used with a SiO_2 as the substrate insulator. Next, a NiCrSi thin-film resistor (TFR) is patterned using a liftoff technique. A plasma enhanced CVD (PECVD) Si_3N_4 dielectric barrier material is then deposited. Contact openings in the dielectric barrier are dry etched, followed by a liftoff of sputtered GeTe. Deposition is done in a Perkin Elmer production deposition tool, and a similar procedure was used to optimize the DC magnetron sputtering parameters of GeTe as done in [11]. Contact and interconnect metallization composed of Ti/Au is then patterned via liftoff, followed by deposition of an additional PECVD Si_3N_4 dielectric passivation with dry etched openings. A second level Au interconnect metallization is then plated to decrease line resistance and allow the formation of air bridges. The wafer is then thinned, and through-substrate vias are dry etched using an inductively-coupled plasma process, before a backside ground plane is Au-plated, establishing ground vias to the front side of the wafer. The plated interconnect metallization and backside processing represent a traditional III-V process flow, and demonstrate the ability of the IPCS devices to be integrated with either a silicon or III-V process flow.

III. Results

A. Material & Device Characterization

Germanium telluride is used as the PCM in this device, as it possesses the lowest crystalline state resistivity relative to other chalcogenides typically used as PCMs [12]. The measured recrystallization temperature for the optimized film was 185°C, with a measured resistivity of $3.6\text{x}10^{-6}$ Ω·m.

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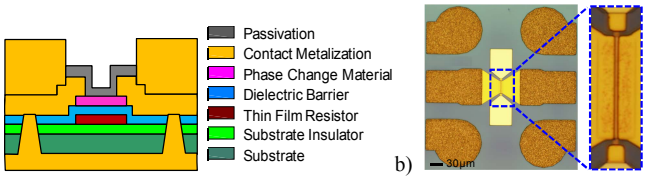

Fig. 1. a) schematic cross-section of the IPCS fabrication process b) optical view of fabricated IPCS SPST using a microstrip design, with a close-up of the IPCS switch area

Using the fabrication process described, various layouts of the IPCS were fabricated with PCS lengths ranging from 0.9 to 2.5-μm, PCS widths ranging from 10 to 30-μm, and TFR widths ranging from 0.5 to 2.5-μm. Fig. 1(b) shows a fabricated single-pole, single-throw (SPST) switch utilizing a microstrip design, with a magnified view of the IPCS area. All devices are pulsed with an HP8114A pulse generator, utilizing a 10-ns rise and fall time. Fig. 2 shows an IPCS device cycled for 100 pulses, using alternating ON and OFF pulses. A 100-ns voltage pulse was used to set the device in the OFF-state, and a 1500-ns voltage pulse was used to set the switch in the ON-state. The switch had an initial ON-resistance of 1.2 Ω, but stabilized to 0.9 Ω after 5 cycles.

B. RF & DC Results

Table I lists the device dimensions, measured ON and OFF resistance, threshold voltage (V_{th}), OFF-capacitance, and calculated cutoff frequency (F_{co}) for 3 different IPCS configurations. It is observed that the OFF-capacitance increases with increasing TFR width, which is consistent with RF simulations. This increase in OFF-capacitance is due to the parasitic capacitance between the interconnect metallization/GeTe and the TFR. As reported in previous publications, the cutoff frequency (F_{co}) is used as the figure of merit, which is defined as the ratio of off-impedance to on-impedance: $1/(2\pi \cdot R_{on} \cdot C_{off})$. By optimizing device geometry and pulse parameters to minimize R_{on} and C_{off}, an F_{co} of 12.5 THz was achieved. This represents the highest reported value for chalcogenide switches to date. Fig. 3 shows the measured and modeled insertion loss and isolation for the 12.5 THz switch. The insertion loss measured less than 0.25dB from 0-40 GHz, and measured 0.15dB at 18 GHz. The third-order intercept (IP3) for all 3 devices measured 72 dBm in the ON-state. The measured isolation was 15 dB at 18 GHz, primarily attributed to the parasitic capacitance through the TFR. The OFF-capacitance for these devices was extracted from the

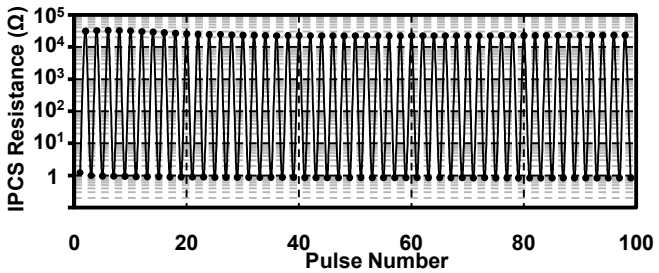

Fig. 2. Measured resistance of the 12.5 THz IPCS device as a function of pulse number, using alternating ON and OFF pulses for 100 pulses. A 100-ns pulse was used to set the device in the OFF-state, and a 1500-ns pulse was used to set the switch in the ON-state

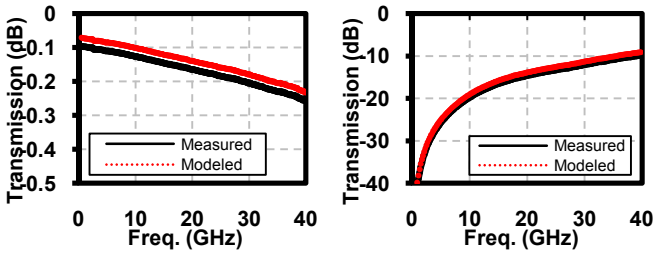

Fig. 3. Measured and modeled (left) insertion loss (ON-state transmission) and (right) isolation (OFF-state transmission) for a 12.5 THz SPST IPCS with 0.9um PCS length and 30um PCS width.

TABLE I
GeTe IPCS Measured Results

IPCS Length	TFR Width	IPCS Width	R_{ON} (Ω)	R_{OFF} (kΩ)	V_{TH} (V)	C_{OFF} (fF)	F_{CO} (THz)
0.9um	0.9um	30um	0.90	26.9	2.09	14.1	12.5
0.9um	1.3um	30um	0.92	31.5	2.72	16.5	10.5
0.9um	1.7um	30um	0.91	35.3	3.31	18.2	9.6

measured isolation with the TFR contact pads floating (disconnected from the pulse generator). This is done intentionally, as the connection of the TFR pads to an unknown load can lead to inconsistent and incorrect extractions of the OFF-capacitance on 2-port structures. Fig. 4 shows the switch response when the TFR pads are shorted to ground. The isolation of the 2-port IPCS SPST with a grounded TFR is significantly higher, due to reduced capacitive coupling through the TFR. The energy that normally couples from port 1 to port 2 through the TFR is partially reflected and partially dissipated in the TFR, increasing the overall isolation at the expense of some increased insertion loss. This could potentially lead to a false assumption in the cutoff frequency and improper evaluations of the switch, as the lower isolation at port-2 (due to the shunt element) decreases the perceived extracted OFF-capacitance by more than 110%, as seen in Table II.

C. RF Circuit Results

Fig. 5 shows a measured SPDT switch with a microstrip design in comparison to other switch technologies from 0-18 GHz [13]-[17]. Fig. 5(a) shows the insertion loss measuring

TABLE II
Measured IPCS Devices With Floating & Grounded TFR Contacts

TFR Contacts	IPCS Length	TFR Width	IPCS Width	R_{ON} (Ω)	C_{OFF} (fF)	F_{CO} (THz)
Floating	0.9um	0.9um	20um	1.41	15.2	7.5
Grounded	0.9um	0.9um	20um	1.40	7.2	15.8

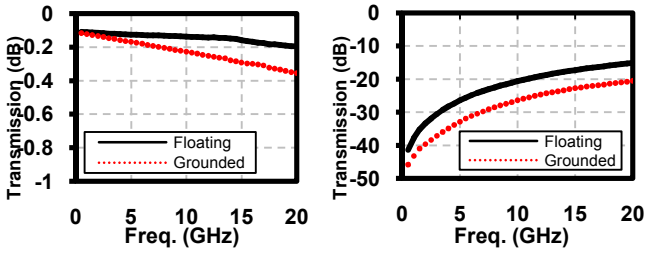

Fig. 4. Measured a) insertion loss (ON-state transmission) and b) isolation (OFF-state transmission) for the two different heater configurations. It is worth noting the two measured switches were 20um in IPCS width, as opposed to the switches in Table I that were 30um wide

less than 0.3dB from 0-18GHz, and Fig. 5(b) shows the isolation measuring greater than 35dB across the band [18].

IV. Conclusion

Advances in the fabrication and design of GeTe-based IPCS switches have decreased the R_{on} and C_{off} to 0.9Ω (0.027 Ω·mm) and 14.1 fF, respectively. This results in an F_{co} of 12.5THz for an SPST switch, which represents a 10x improvement over first generation IPCS devices. These devices have been integrated into an SPDT RF switch that measures less than 0.25dB insertion loss from 0-18GHz, and greater than 35dB of isolation across the same band, demonstrating the ability to fabricate non-volatile IPCS MMICs such as SPDTs, tunable filters, phase shifters, time delay units, and multi-port switch matrices. Future work, already in progress, focuses on improved processes and materials to decrease RF losses and power consumption, and further increase the threshold voltage.

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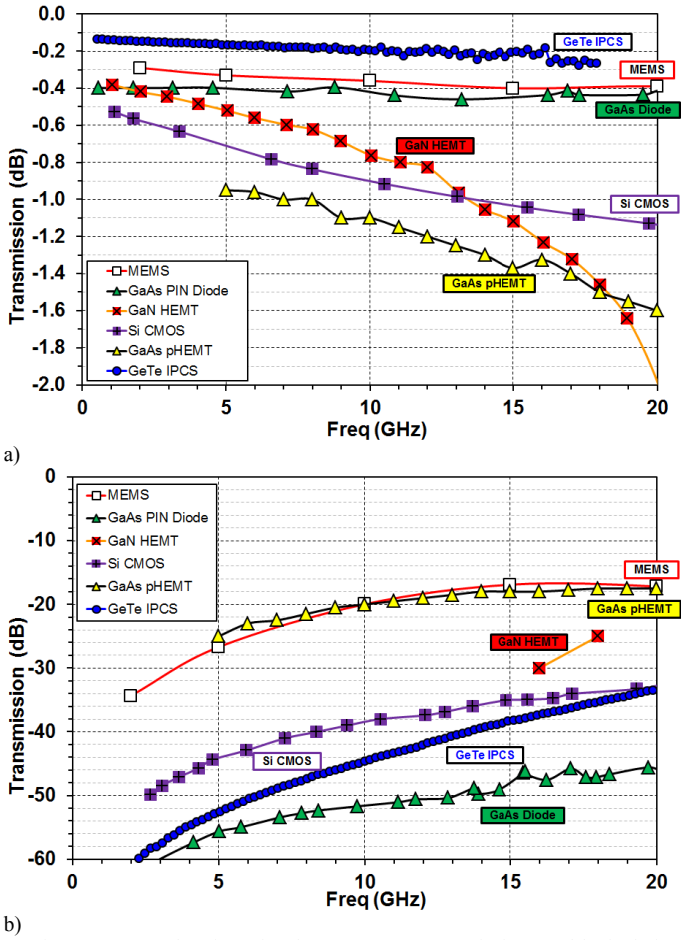

Fig. 5. Measured a) insertion loss (ON-state transmission) and b) isolation (OFF-state transmission) for the fabricated SPDT switch, with comparisons to other technologies [13]-[17]

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A 3/5 GHz Reconfigurable CMOS Low-Noise Amplifier Integrated with a Four-Terminal Phase-Change RF Switch

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Abstract

This paper presents the first reported *in-situ* reconfiguration of a narrowband CMOS low noise amplifier (LNA) over two widely separated frequency bands using a GeTe phase-change (PC) switch. Previous work has demonstrated the attractiveness of CMOS-PC integration to realize high-performance reconfigurable RF front-end circuits [1-2]. Four-terminal PC switches with small form factor have been recently shown to possess close-to-ideal properties of an RF switch: a high OFF/ON resistance ratio and extremely high figure-of-merit for RF switches ($F_{CO} = 1/(2\pi R_{ON}C_{OFF})$) [3-4]. In this work, we present a robust realization of a reconfigurable 3/5 GHz LNA designed and fabricated in a 0.13 µm CMOS process and flip-chip integrated with a four-terminal PC switch fabricated using an in-house process.

PC Switch Structure and Operation

An isometric view and an SEM picture of the four terminal PC switch [3] is shown in Fig. 1, having two RF terminals (signal) and two heater terminals (control signal). The length and width of the transformable PC material (GeTe) in the RF gap were designed to be ~500-600 nm and 20 µm respectively to achieve a low R_{ON} in the crystalline phase. Two key innovations are introduced in this work to enhance robustness and reduce parasitic capacitance. First, a tungsten heating element of width 1 µm and length 25 µm is used to transform the PC material between the crystalline (on) and amorphous (off) phases. Compared to NiCrSi [3-4], the higher melting temperature and lower resistivity of W enables a more reliable heater that can switch the PC material using lower pulse voltages. Second, the heater is electrically isolated from the PC material using 100 nm of AlN as the dielectric barrier. Compared to Si_3N_4, used as a barrier in [3-4], the high thermal conductivity of AlN (285 W/(m.K) [5]) enables heat to flow from the heater to the PC material without forming a large temperature gradient between the RF signal path and the heater.

To turn the switch off, a 100 ns wide voltage pulse (Fig. 2(e)) is applied to the heater to raise the temperature

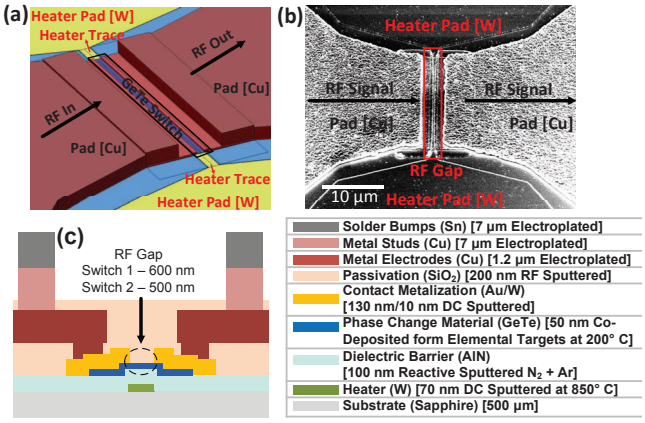


Fig. 1: (a) Isometric view, (b) SEM photo, and (c) layer stack of the PC chip (not drawn to scale) including the bump bonds. Layer materials and thicknesses are indicated.

of the PC material above the melting temperature (T_M), after which the temperature quickly falls, quenching in the amorphous (high resistivity) state of the PC material in the RF gap. To turn the switch on, a 1 µs wide lower voltage pulse is applied to the heater to raise the PC material slightly above the crystalline temperature (T_C) in order to crystallize the material in the RF gap.

PC Switch Fabrication and Integration

The designed PC switch was fabricated in a custom process. A cross section of the layer stack is shown in Fig. 1(c) with all process steps noted. The PC material (Ge_xTe_{1-x}) was co-sputtered from elemental targets at 200°C. The composition ratio of the GeTe alloy was optimized near 50/50 to achieve a very low resistivity of 1.83×10^{-6} Ω-m.

Four PC chips were fabricated and flip-chip bonded to CMOS LNAs. The first two chips contained a standard PC switch with designed RF gaps of 600 nm (Chip #1) and 500 nm (Chip #2). Fig. 2 shows the measured R_{ON} and off-state parasitics (R_{OFF}, C_{OFF}) of similar standalone PC switches extracted from 1-port S-parameter measurements. The cut-off frequency, F_{CO}, for the two switches are 5.5 THz and 6.4 THz, respectively. The third and fourth chips were designed to serve as control

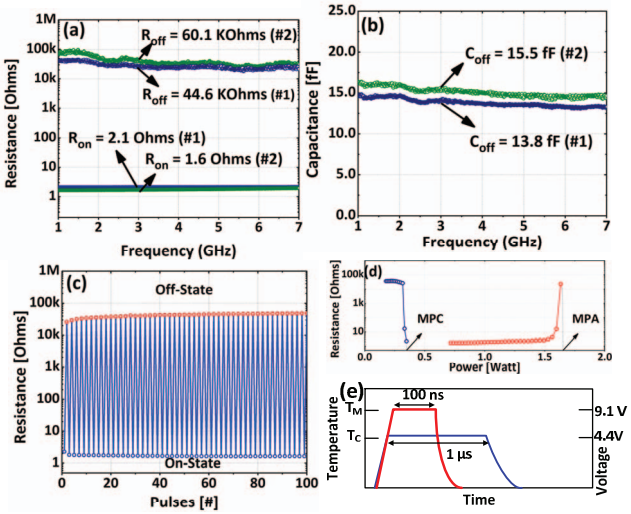


Fig. 2: Stand-alone measurements of two fabricated PC switches (#1, #2): (a) R_{ON} and R_{OFF} (b) C_{OFF} (c) demonstration of switching behavior for 100 cycles of #2, (d) characterization of minimum power to amorphize (MPA) and minimum power to crystallize (MPC) of #2, and (e) heat and voltage profiles of the amorphization (red) and crystallization (blue) pulse with 10 ns rise and fall times.

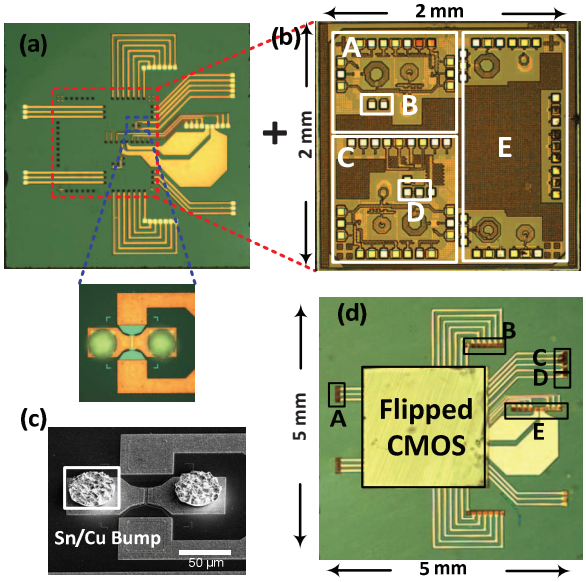


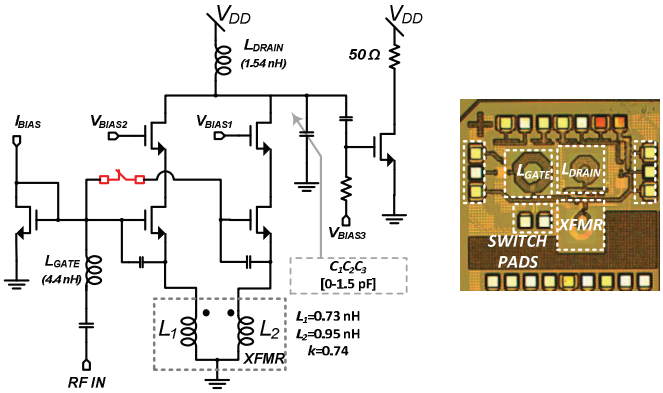
Fig. 3: Die photos of (a) PC chip and (b) CMOS chip. (c) SEM picture of PC switch (d) Die photo of integrated chip. In (b): A – LNA with flip-chip pads for integration with PC chip, B – flip-chip pads to connect to the PC switch, C – baseline LNA with ideal short for 3 GHz testing, D-shorted flip-chip pads, E – stand-alone test structures. In (d): A – RF out [GSG probe], B – power/bias pads [eye-pass probe], C – RF input [GSG probe], D – heater pads, E – control signal pads [eye-pass probe].

experiments, wherein the PC material was removed from the RF gap and replaced with Au (Control Chip #1) or nothing (Control Chip #2) to represent an ideal short and ideal open, respectively. Figure 3 shows the die photographs and dimensions of the PC chip, the CMOS chip and flip-chip bonded chip.

LNA Design

The circuit schematic and the principle of operation of the LNA are shown in Figs. 4 and 5 respectively. The LNA comprises two inductively-generated cascode common-source (CS) legs, with one leg (both legs) turned on in the 5 GHz (3 GHz) mode. In contrast to a conventional LNA, finite coupling is introduced between the two source inductors, enabling reconfiguration using a single PC switch. The PC switch, inserted between the gate inductor and one of the CS stages, removes it from the input signal path when turned off during operation in the higher band (F_H =5 GHz). To enable the lower band operation (F_L =3 GHz), the PC switch is turned on and both CS stages are included in the signal path.

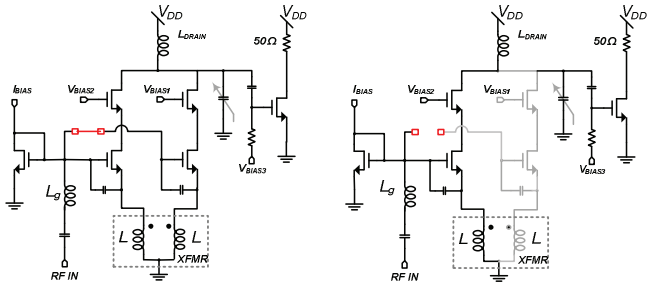
It is important to note that a CMOS switch cannot replace the PC switch that is used to reconfigure the input matching network across the two modes. This is because the switch appears directly in the RF signal path before the gate of the LNA transconductors, and must therefore have a very low R_{ON} to avoid degrading the LNA's noise figure (NF). R_{ON} values comparable to those of the PC switch



(a) (b)

Fig. 4: (a) Circuit Schematic of the 3/5 GHz LNA (b) Die photo of the LNA in 0.13 µm CMOS.

necessitate very wide CMOS switches resulting in parasitic drain and source capacitances to the substrate and the transistor gate terminal of the order of several hundred femtofarads. This is consistent with the observation that for similar R_{ON}, PC switches exhibit a significantly higher F_{CO} [2] (30.6 THz for a 0.8 Ω GeTe-via switch vs. 0.25 THz for a 0.13 µm CMOS switch). The shunt parasitics from the CMOS switch also change the effective input impedance in both the modes considerably, leading to poor matching and reduced gain.



$$F_L = \frac{1}{2\pi\sqrt{(L+M+2L_g)C_{gs}}} \qquad F_H = \frac{1}{2\pi\sqrt{(L+L_g)C_{gs}}}$$

Fig. 5: (a) Operation in 3 GHz with PC switch turned on (b) Operation in 5 GHz mode with PC switch turned off. F_L and F_H are the lower band and higher band center frequencies in terms of L_g, the gate inductance, C_{gs}, the gate to source capacitance of the input transistor, L, the self-inductance, and M, the mutual inductance of the source transformer.

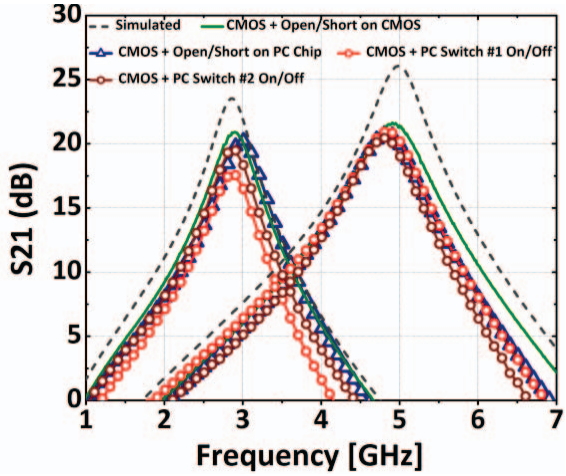


Fig. 6: Post-layout simulated and measured LNA S21 in 3/5 GHz modes of (1) baseline CMOS LNAs, (2) control LNAs and (3) two CMOS-PC LNAs. In each mode, all chips were biased identically. The buffer gain and the traces on the PC chip were not de-embedded from the final measurement results.

A capacitor bank, controlled by a three-bit digital word $C_1C_2C_3$, is placed at the output to switch the output tank's resonant frequency and the LNA S_{21} between the 3 GHz ($C_1C_2C_3$ = '111') and 5 GHz ($C_1C_2C_3$ = '000') modes. The size and R_{ON} of the CMOS switches in the capacitor bank poses a trade-off between the output tank's quality factor and the off-state capacitance. However, wide CMOS switches can be employed in the capacitor bank by ensuring that the off-state capacitance is accounted for during operation in the 5 GHz mode.

To obtain baseline CMOS measurements in each mode, separate CMOS LNA's were fabricated in the two configurations (Fig. 3(b)). The configuration with open

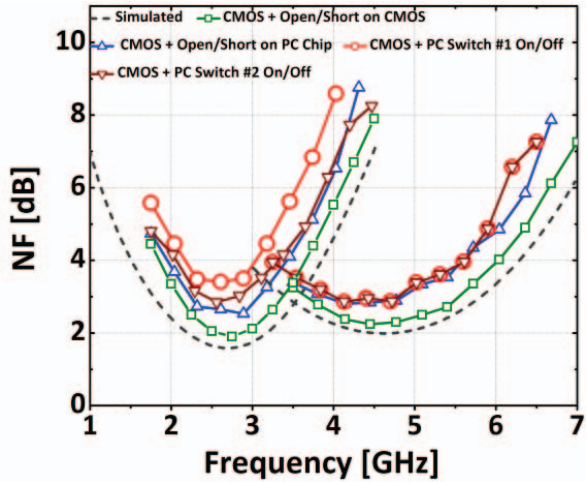


Fig. 7: Post-layout simulated and measured LNA NF in 3/5 GHz modes. NFs of the CMOS-PC chips were measured after 6 switching cycles.

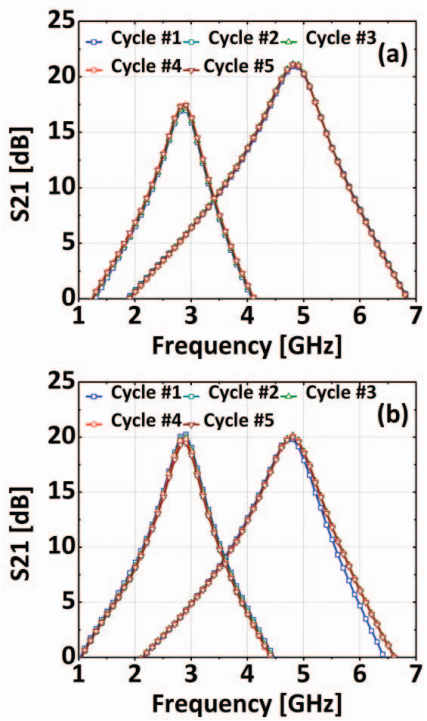


Fig. 8: Measured S21 over 5 switching cycles (a) Chip #1 (b) Chip #2

flip-chip pads was used for 5 GHz testing and for bonding with the PC chip. The configuration with shorted flip-chip pads was used for 3 GHz mode testing.

Experimental Results

S_{21} and NF measurements on: (1) baseline CMOS LNA's, (2) control LNAs and (3) two CMOS-PC LNAs are shown in Figs. 6 and 7 respectively. The overall S_{21} includes the output buffer gain (~0.95 when driving 50 Ω). The

Table I – Performance summary of all LNAs

	Band [GHz]	Peak S_{21} [dB]	Min NF [dB]	Power* [mW]
Baseline Chip #1: CMOS Only	3	20.6	1.9	7.2
Baseline Chip #2: CMOS Only	5	21.6	2.25	3.6
Control Chip #1: CMOS + Short on PC	3	20.2	2.55	7.2
Control Chip #2: CMOS + Open on PC	5	20.8	2.8	3.6
Chip #1: CMOS + PC	3	17.5	3.41	7.2
	5	20.9	2.86	3.6
Chip #2: CMOS + PC	3	19.5	2.85	7.2
	5	20.1	2.86	3.6

* Power consumption of the core LNA (excluding the buffer) from a 1.2 V supply. Power drawn by the output buffer is 8.4 mW.

CMOS-PC LNA Chip #2 achieves a peak conversion gain of 19.5 dB (20.1 dB) and a minimum NF of 2.85 dB (2.86 dB) in the 3 GHz (5 GHz) band. These metrics compare favorably to the measured performance metrics of the baseline CMOS LNAs, and to previously published non-reconfigurable 3 GHz and 5 GHz CMOS LNAs [6]. For the CMOS-PC LNA Chip #1, a higher NF and a lower gain in the 3 GHz band were observed. This is due to increased contact resistance between the solder bumps and the aluminum bond pads on the CMOS chip due to a weak solder joint. Table I summarizes the performance of all the LNAs. The performance of the LNA was also characterized over 5 PC on/off cycles by measuring the S_{21} after each cycle. As shown in Fig. 8, the S_{21} remains constant in the two bands suggesting stable and reversible transformations.

Conclusion

In this work, a dual-band CMOS LNA, reconfigurable through a four terminal phase-change (PC) switch, is demonstrated. An RF PC switch with low parasitics and high cut-off frequency was designed, fabricated and integrated with a CMOS LNA. Minimal performance degradation was observed from the overhead of the flip-chip integration. This work demonstrates that by using PC RF switches, tuned CMOS circuits can be stably and reversibly reconfigured across wide frequency ranges, while simultaneously achieving RF performance approaching that of non-reconfigurable CMOS circuits. This work further highlights the promise of PC switches as an enabling technology for complex field-programmable transceivers.

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